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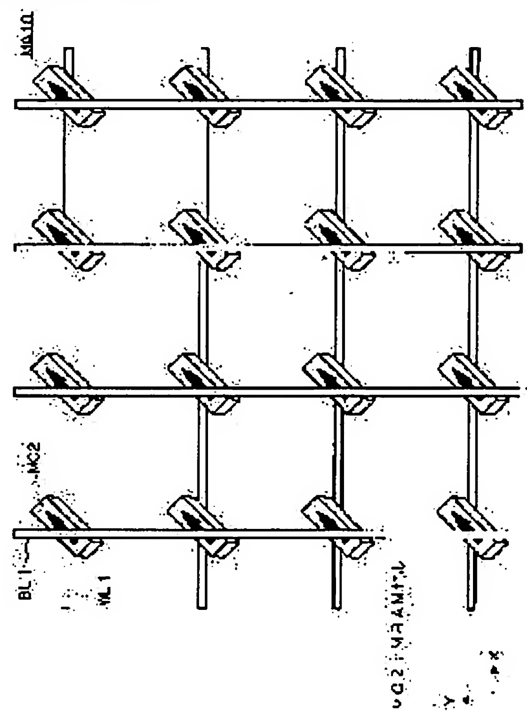
(54) MAGNETIC STORAGE SYSTEM AND MAGNETIC SUBSTRATE

(57)Abstract:

PROBLEM TO BE SOLVED: To provide a RAM requiring lower power dissipation in writing and time in erasing and writing.

SOLUTION: A plurality of bit wires BL1 disposed in parallel each other are disposed so that they are intersecting over a plurality of word wires WL1 disposed in parallel each other. MRAM cells MC2 are formed at each intersection point sandwiched between the word wires and the bit wires. Each MRAM cell MC3 is disposed so that easy axes indicated by arrows are inclined at 45-degree to the bit and word wires.



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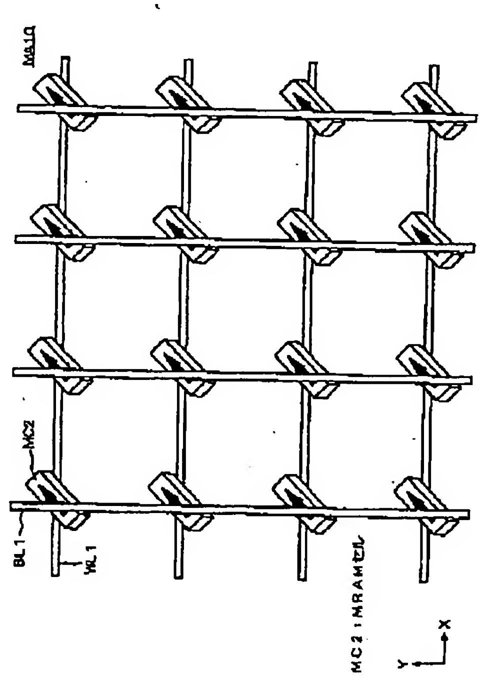
(54)【発明の名称】 磁気記憶装置および磁性体基板

(57)【要約】
【課題】 書き込み時の消費電力を低減したＭＲＡＭを提供するとともに、消去および書き込みに費やす時間を低減したＭＲＡＭを提供する。
【解決手段】 互いに平行に配設された複数のワード線ＷＬ１の上部において交差するように、互いに平行に配設された複数のビット線ＢＬ１が配設されている。そして、ワード線およびビット線で挟まれる各交点にＭＲＡＭセルＭＣ２が形成されている。そして、矢印で示すイージーアクシスが、ビット線およびワード線に対して４５度傾くように各ＭＲＡＭセルＭＣ３が配設されている。



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CLAIMS

[Claim(s)]
[Claim 1] Two or more bit line and two or more word lines which cross by non-contact and constitute a matrix, It is arranged by the intersection of said two or more bit lines and said two or more word lines, respectively. It is the magnetic storage equipped with two or more memory cells containing at least one magnetic tunnel junction. Said two or more memory cells It is arranged, respectively between [of said two or more bit lines] 1 and 1 of said two or more word lines. Said at least one magnetic tunnel junction It has the software ferromagnetic layer which can change the direction of magnetization. Said at least one magnetic tunnel junction Magnetic storage arranged so that the easy axis which is the easy direction of magnetization of said software ferromagnetic layer may have the include angle of 40 - 50 degrees to the extension direction of said two or more bit lines and two or more of said word lines.
[Claim 2] Said magnetic tunnel junction is magnetic storage according to claim 1 with which a plane view configuration is constituted by the rectangle so that the side parallel to said easy axis may become longer than the side which intersects perpendicularly with said easy axis.
[Claim 3] Two or more bit line and two or more word lines which cross by non-contact and constitute a matrix, It is arranged by the intersection of said two or more bit lines and said two or more word lines, respectively. It is the magnetic storage equipped with two or more memory cells containing at least one magnetic tunnel junction. It connects with the 1st edge of two or more of said bit lines, respectively. The electric connection between said 1st edge and the 1st power source [2nd] of power-source ****** Two or more 1st switchable change means, Magnetic storage which is connected to the 2nd edge of two or more of said bit lines, respectively, and is equipped with two or more 2nd switchable change means for the electric connection between said 2nd edge and said 1st power source [2nd] of the power-source ****** above.
[Claim 4] As for said 1st change means, each 1st main electrode is connected to the 1st edge of two or more of said bit lines. Each 2nd main electrode has the 1st and 2nd MOS transistors of the same conductivity type connected to said the 1st power source and said 2nd power source. Said 2nd change means Magnetic storage according to claim 3 which has 4 MOS transistors of the 3rd and ** of the same conductivity type by which each 1st main electrode was connected to the 2nd edge of two or more of said bit lines, and each 2nd main electrode was connected to said the 1st power source and said 2nd power source.
[Claim 5] As for said 1st change means, each 1st main electrode is connected to the 1st edge of two or more of said bit lines. Each 2nd main electrode has the 1st and 2nd MOS transistors of differing of the conductivity type connected to said the 1st power source and said 2nd power source. Said 2nd change means Magnetic storage according to claim 3 which each 1st main electrode is connected to the 2nd edge of two or more of said bit lines, and has the 3rd and 4th MOS transistors from which the conductivity type by which each 2nd main electrode was connected to said the 1st power source and said 2nd power source differs.
[Claim 6] Said 1st and 2nd MOS transistors each Said 2nd MOS transistor connected between the main electrodes of the above 1st, and the 5th MOS transistor of the same conductivity type, The 3rd and 4th

MOS transistors of an account each Said 4th MOS transistor connected between the main electrodes of the above 1st, and the 6th MOS transistor of the same conductivity type, It is the magnetic storage according to claim 5 by which the control electrode of said 5th and 6th MOS transistors is connected to the 3rd power source which gives the predetermined electrical potential difference which will always be in an ON state by preparing for a pan.
[Claim 7] Two or more bit line and two or more word lines which cross by non-contact and constitute a matrix, and it being arranged by the intersection of said two or more bit lines and said two or more word lines, respectively, and with two or more memory cells containing at least one magnetic tunnel junction, and two or more memory cell arrays come out of and constituted Two or more main word lines crossed to said two or more memory cell arrays, and two or more memory cell array selection lines arranged corresponding to each of two or more of said memory cell arrays, It has the memory cell array group of at least 1 the bottom. **** -- said two or more word lines It connects with the output of the 1st combination logic gate established in the intersection of said two or more main word lines and two or more of said memory cell array selection lines, respectively, respectively. The input of said 1st combination logic gate is magnetic storage connected to 1 of said two or more main word lines in a crossover condition, and 1 of said two or more memory cell array selection lines.
[Claim 8] Two or more global word lines which have two or more said memory cell array groups of at least 1, and are crossed to said two or more memory cell array groups, It has further two or more memory cell array group-selection lines arranged corresponding to each of two or more of said memory cell array groups. Said two or more main word lines It connects with the output of the 2nd combination logic gate established in the intersection of said two or more global word lines and two or more of said memory cell array group-selection lines, respectively, respectively. The input of said 2nd combination logic gate is magnetic storage according to claim 7 connected to 1 of said two or more global word lines in a crossover condition, and 1 of said two or more memory cell array group-selection lines.
[Claim 9] Two or more bit line and two or more word lines which cross by non-contact and constitute a matrix, and it being arranged by the intersection of said two or more bit lines and said two or more word lines, respectively, and with two or more memory cells containing at least one magnetic tunnel junction, and two or more memory cell arrays come out of and constituted Had two or more Maine bit lines crossed to said two or more memory cell arrays, and two or more memory cell array selection lines arranged corresponding to each of two or more of said memory cell arrays. It has the memory cell array group of at least 1. Said two or more bit lines It connects with the output of the 1st combination logic gate established in the intersection of said two or more Maine bit lines and two or more of said memory cell array selection lines, respectively, respectively. The input of said 1st combination logic gate is magnetic storage connected to 1 of said two or more Maine bit lines in a crossover condition, and 1 of said two or more memory cell array selection lines.
[Claim 10] Two or more global bit lines which have two or more said memory cell array groups of at least 1, and are crossed to said two or more memory cell array groups, It has further two or more memory cell array group-selection lines arranged corresponding to each of two or more of said memory cell array groups. Said two or more Maine bit lines It connects with the output of the 2nd combination logic gate established in the intersection of said two or more global bit lines and two or more of said memory cell array group-selection lines, respectively, respectively. The input of said 2nd combination logic gate is magnetic storage according to claim 9 connected to 1 of said two or more global bit lines in a crossover condition, and 1 of said two or more memory cell array group-selection lines.
[Claim 11] Two or more bit line and two or more word lines which cross by non-contact and constitute a matrix, and it being arranged by the intersection of said two or more bit lines and said two or more word lines, respectively, and with two or more memory cells containing at least one magnetic tunnel junction, and the memory cell array come out of and constituted It is the magnetic storage which generates a field in the direction in alignment with the easy axis which is the direction for magnetization of said software ferromagnetic layer where have an inductor, said at least one magnetic tunnel junction has the software ferromagnetic layer which can change the direction of magnetization, and said inductor is easy.
[Claim 12] It is the magnetic storage according to claim 11 which is the coiled form inductor arranged

by arranging said at least one magnetic tunnel junction so that said easy axis may agree in the extension direction of said two or more bit lines or two or more of said word lines so that said inductors might surround said memory cell array along the extension direction of said two or more bit lines or said two or more word lines which agree with the direction of said easy axis.
[Claim 13] Two or more bit line and two or more word lines which cross by non-contact and constitute a matrix, and it being arranged by the intersection of said two or more bit lines and said two or more word lines, respectively, and with two or more memory cells containing at least one magnetic tunnel junction, and at least one memory cell array come out of and constituted It is prepared in the outside of said two or more bit lines and said two or more word lines of said at least one memory cell array, respectively. Magnetic storage equipped with at least one wrap plate-like flash plate bit line and at least one flash plate word line for the formation field of said two or more bit lines and two or more of said word lines.
[Claim 14] It is the magnetic storage according to claim 13 by which two or more arrangement is carried out, respectively by having two or more said at least one memory cell arrays, and arranging said two or more memory cell arrays in the shape of a matrix so that said at least one flash plate bit line and at least one flash plate word line may constitute a matrix in accordance with the array of two or more of said memory cell arrays.
[Claim 15] Two or more bit line and two or more word lines which cross by non-contact and constitute a matrix, and it being arranged by the intersection of said two or more bit lines and said two or more word lines, respectively, and with two or more memory cells containing at least one magnetic tunnel junction, and the memory cell array come out of and constituted Even if there are few said two or more bit lines and two or more word lines, it is arranged in two edges of the method of one, respectively. Magnetic storage equipped with at least one inductor which saves the current of the selected bit line and a word line which flows to the method of one at least by LC resonance, and at least one capacitor.
[Claim 16] It has two or more said at least one inductors and said at least one capacitors. Said two or more bit lines Two become a pair and two or more bit line pairs are constituted. Said two or more inductors Corresponding to said two or more each of a bit line pair, two or more 1st inductors arranged so that it might connect electrically between bit lines are included. Said two or more capacitors Magnetic storage according to claim 15 which contains two or more 1st capacitors electrically connected corresponding to each of two or more of said bit lines in an edge opposite to the arrangement side of two or more of said inductors.
[Claim 17] Two become a pair and said two or more word lines constitute two or more WORD line pairs. Said two or more inductors Corresponding to each of two or more of said WORD line pairs, two or more 2nd inductors arranged so that it might connect electrically between word lines are included further. Said two or more capacitors Magnetic storage according to claim 16 which contains further two or more 2nd capacitors electrically connected corresponding to each of two or more of said word lines in an edge opposite to the arrangement side of two or more of said inductors.
[Claim 18] At least one semiconductor chip and the screen which consists of conductors and contains said at least one semiconductor chip, The package which consists of resin and contains said screen, and the base substrate which closes and seals opening of said package, With the bump for signal transmissions who is arranged in the outside principal plane of said base substrate, and performs the signal transmission of said at least one semiconductor chip and exterior It is arranged so that said bump for signal transmissions may be surrounded, and it has the bump for electric shielding electrically connected to said screen. Said at least one semiconductor chip Magnetic storage including the magnetic storage chip equipped with the memory cell array constituted by having two or more memory cells containing at least one magnetic tunnel junction.
[Claim 19] Magnetic storage according to claim 18 further equipped with the 1st stress relaxation film arranged in the inside and the outside of the opening edge of said screen, and the 2nd stress relaxation film arranged by the wall of said screen.
[Claim 20] Said account chip of the MAG and said circuit chip are magnetic storage according to claim 19 which piles up up and down and is contained by said electric shielding inside of the body, including further the circuit chip in which said at least one semiconductor chip includes the circumference circuit

of said memory cell array.
[Claim 21] Said at least one magnetic tunnel junction is magnetic storage according to claim 18 with which said screen consists of ferromagnetics which have said software ferromagnetic layer and EQC, and bigger permeability than it by having the software ferromagnetic layer which can change the direction of magnetization.
[Claim 22] Said screen is magnetic storage according to claim 18 which consists of the antiferromagnetic substance.
[Claim 23] Said screen is magnetic storage according to claim 18 which consists of multilayers of a ferromagnetic and the antiferromagnetic substance.
[Claim 24] The magnetic-substance substrate which was arranged throughout the principal plane and which has at least the multilayers which form at least one magnetic tunnel junction.
[Claim 25] Said multilayers are magnetic-substance substrates according to claim 24 which contain the diamagnetic-material layer, the ferromagnetic layer, the tunnel barrier layer that consists of insulators, and software ferromagnetic layer which were arranged in order as said at least one magnetic tunnel junction.
[Claim 26] Said multilayers are magnetic-substance substrates according to claim 25 which are arranged by the lower part of said at least one magnetic tunnel junction, and contain further the two-layer film of the 1st conductivity-type impurity layer and the 2nd conductivity-type impurity layer which constitute pn junction.
[Claim 27] Said magnetic-substance substrate is a magnetic-substance substrate according to claim 24 which has said multilayers on a SOI substrate equipped with the substrate section used as a foundation, and the SOI layer which was arranged on this substrate section, and which embedded and was arranged on the oxide film and this embedding oxide film.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] Especially this invention relates to magnetic storage with the non-volatile memory array which uses a magnetic tunnel junction as each memory cell about magnetic storage.
[0002]
[Description of the Prior Art] The structure which sandwiched the <tunnel magneto-resistive effect> insulator with two ferromagnetics is called a magnetic tunnel junction (Magnetic TunnelJunction:MTJ).
[0003] The conceptual diagram of MTJ is shown in drawing 67 . In drawing 67 , it is arranged so that an insulating layer TB may be sandwiched by the ferromagnetic layers FM21 and FM22, and it has become the ferromagnetic layers FM21 and FM22 with the configuration that an electrical potential difference is impressed.
[0004] In this structure, measurement of the current which tunnels an insulating layer TB observes the phenomenon in which a current value changes with sense of magnetization of two ferromagnetic layers.
[0005] This phenomenon is called the tunnel magnetic-reluctance (Tunnel Magnetic Resistance:TMR) effectiveness. The TMR effectiveness is explained using drawing 68 - drawing 70 .
[0006] Drawing 68 shows the mimetic diagram of the density of states N of transition metals (E). In drawing 68 , a density of states is shown on an axis of abscissa, Energy E is shown on an axis of ordinate, and the electron which an atom has is classified according to the sense of spin, and is shown. That is, the density of states of the atom with which the sense of spin has a downward electron on left-hand side toward drawing 68 is shown, and the density of states of the atom with which the sense of spin has a upward electron on right-hand side is shown.
[0007] Moreover, in drawing 68 , in order to show typically the atom with which it fills up with the electron to Fermi level among 3d orbit and 4 s orbits, hatching shows the atom with which it fills up with the electron to Fermi level bordering on Fermi level.
[0008] Transition metals become a ferromagnetic because the number of upward spin differs from the number of downward spin in the electron of 3d orbit among the atoms with which it fills up with the electron to Fermi level.
[0009] That is, since the electron of 4 s orbits has the number the same as the number of upward spin of downward spin, it is not contributed to magnetic generating.
[0010] Drawing 69 and drawing 70 are drawings showing the TMR effectiveness typically. In drawing 69 , since there are more atomic density of stateses which have the electron of downward spin among 3d orbits of the atom which constitutes the ferromagnetic layer FM 21 on the left-hand side of an insulating layer TB than the atomic density of states which has the electron of upward spin, the sense of magnetization becomes downward as a whole.
[0011] The sense of as a whole [same] magnetization of the ferromagnetic layer FM 22 on the right-hand side of an insulating layer TB becomes downward.
[0012] Electronic tunneling happens so that the sense of the spin of ****** and a final state may mainly be saved. Since both the downward spin state consistencies of ****** (inside of the ferromagnetic layer

FM 21) and a final state (inside of the ferromagnetic layer FM 22) are large in the case of drawing 69 , a tunnel probability becomes large and tunnel current also becomes large. That is, tunnel magnetic reluctance becomes small.
[0013] On the other hand, although the atomic density of states which has the electron of the upward spin of ****** (inside of the ferromagnetic layer FM 21) is large in drawing 70 , since the atomic density of states which has the electron of the upward spin of a final state (inside of the ferromagnetic layer FM 22) is small, a tunnel probability becomes small and tunnel current also becomes small. That is, tunnel magnetic reluctance becomes large.
[0014] When resistance in the case of having turned to RF and an opposite direction for resistance when the sense of magnetization of two ferromagnetic layers is mutually the same here is set to RAF, tunnel magnetic-reluctance rate of change (Tunnel Magnetic Resistance Rate:TMRR) is expressed with a degree type.
[0015]
[Equation 1]

$$TMRR=\frac{R_{AF}-R_F}{R_A}=\frac{P_1P_2}{1-P_1P_2}\quad\cdots(1)$$

[0016] In addition, in the above-mentioned formula (1), P1 and P2 are the rates of spin polarization of the ferromagnetic layers FM21 and FM22, respectively.
[0017] And when the density of states in the Fermi surface of sigma spin band is set to Dsigma (EF), the rate of spin polarization is expressed with a formula below.
[0018]
[Equation 2]

$$P=\frac{D_\uparrow(E_F)-D_\downarrow(E_F)}{D_\uparrow(E_F)+D_\downarrow(E_F)}\quad\cdots(2)$$

[0019] That is, the rate of spin polarization becomes so large that the density-of-states difference of the upward spin in a Fermi surface and downward spin is large. Moreover, TMRR becomes large, so that the rate of spin polarization approaches 1. Moreover, it is known that spin polarization is proportional to magnetization. Here, the rate of spin polarization of the various magnetic substance is collectively shown in Table 1.
[0020]
[Table 1]

材料	スピン分極率
Fe	0.44
Co	0.35
Ni	0.23
$Ni_{80}Fe_{20}$	0.25，0.45
FeCo	0.53
NiMnSb	1，0.58
PtMnSb	1
CrO_2	1
Fe_3O_4	1
(La・Sr)MnO_3	1

[0021] The equipment which the magnetization direction of two ferromagnetic layers is made to correspond to 0 or 1, and memorizes data using the TMR effectiveness explained above is MRAM (Magnetic Random AccessMemory).
[0022] Therefore, with the structure of drawing 67 , although only one side of two ferromagnetic layers of MTJ wants to change the magnetization direction, if a field is applied, the direction of magnetization of both ferromagnetic layers may change. Then, as shown in drawing 71 , the structure where the

antiferromagnetic substance layer was formed on one ferromagnetic layer is proposed in order to fix the magnetization direction of one ferromagnetic layer.
[0023] In drawing 71 , an insulating layer TB is inserted in the ferromagnetic layers FM21 and FM22, and the antiferromagnetic substance layer AF is arranged in the upper part of the ferromagnetic layer FM 21. In addition, the positive electrode of DC power supply is connected to the antiferromagnetic substance layer AF, and the negative electrode is connected to the ferromagnetic layer FM 22.
[0024] When a ferromagnetic and the antiferromagnetic substance are formed adjacently, and the magnetic flux which pierces through both closes, the direction of magnetization is fixed. This structure is called a spin bulb mold ferromagnetism tunnel junction component.
[0025] Moreover, the configuration of the modification of a spin bulb mold ferromagnetism tunnel junction component is shown in drawing 72 . In drawing 72 , an insulating layer TB is inserted in the ferromagnetic layers FM21 and FM22, the antiferromagnetic substance layer AF is arranged in the upper part of the ferromagnetic layer FM 21, and the ferromagnetic layer FM 23 is arranged in the lower part of the ferromagnetic layer FM 22.
[0026] Here, although the antiferromagnetic substance layer AF consists of IrMn(s) 20-30atom.% Containing Ir (iridium) and the direction of magnetization of the ferromagnetic layer FM 21 is fixed, since it is better to be hard to reverse the direction of magnetization to an external magnetic field, CoFe with big coercive force as a ferromagnetic layer FM 21 is used.
[0027] Moreover, as explained using the formula (1), since, as for tunnel magnetic-reluctance rate of change (TMRR), the one where the rate of spin polarization is larger becomes large, CoFe is used as an ingredient with the large rate of spin polarization.
[0028] On the other hand, although the same CoFe as the ferromagnetic layer FM 22 is used, the ferromagnetic layer FM 22 is more desirable [the ingredient with small coercive force] so that the direction of magnetization can be controlled by as small the external magnetic field as possible.
[0029] In the configuration of drawing 72 , it is the purpose which make easy to reverse the sense of magnetization of the ferromagnetic layer FM 22, and nickel80Fe20 (permalloy) with coercive force and the rate of spin polarization small as a ferromagnetic layer FM 23 is used. Thereby, the ferromagnetic layer FM 22 can reverse the sense of magnetization by the small external magnetic field.
[0030] Drawing 73 shows the practical structure of the spin bulb mold ferromagnetism tunnel junction component shown in drawing 72 , and drawing 74 shows the observation property of TMR in the structure concerned.
[0031] In drawing 73 , an insulating layer TB is arranged in the layered product upper part of the antiferromagnetic substance layer AF superficially arranged on Substrate BD, and the ferromagnetic layer FM 21, and the ferromagnetic layer FM 23 is arranged in the upper part of an insulating layer TB. In such a configuration, the result of having impressed the external magnetic field and having measured change of magnetic reluctance MR is drawing 74 .
[0032] In drawing 74 , a field (one oersted = it converts by about 79 A/m) is shown on an axis of abscissa, and the tunnel reluctivity (TMRR) is shown on the axis of ordinate. Drawing 74 shows that TMRR has realized 36% of value, that a field required for reversal of the direction of magnetization is as low as about 30 (x79 A/m) extent, and that the symmetrical hysteresis is acquired to the direction of a field.
[0033] the direction of magnetization of two ferromagnetics of the magnetic tunnel junction component which constitutes a memory cell from <structure and the principle of operation> MRAM of MRAM -- the same -- or it becomes in the opposite direction -- as -- an external magnetic field -- controlling -- the direction of magnetization -- the same -- or the condition of an opposite direction is made to correspond to 0 or 1, and data are memorized.
[0034] The memorized data can be read by passing a predetermined current to a memory cell and sensing the both-ends electrical potential difference of tunnel magnetic reluctance. And since it is easy to sense so that the rate (TMRR) of a tunnel magnetic-reluctance value change is large, a ferromagnetic material with the big rate of spin polarization is advantageous for MRAM.
[0035] Moreover, the writing of data should just change the direction of magnetization of one

ferromagnetic into wiring (a word line and bit line) using the field which passed the predetermined current and was generated.

[0036] Structure and actuation are explained as a conventional example of MRAM below <the structure of a MRAM cel> about MRAM currently exhibited with United States patent USP5,793,697.

[0037] Drawing 75 is the perspective view showing a MRAM cel array and a cel. In drawing 75 , bit lines 4, 5, and 6 are mutually arranged in parallel so that it may cross in the upper part of the word lines 1, 2, and 3 arranged in parallel mutually.

[0038] And the MRAM cel (only calling a cel henceforth) 9 is formed in each intersection across which it faces with a word line and a bit line. As drawing 75 is shown as an enlarged drawing, the MRAM cel 9 is the structure where the laminating of the silicon pn junction diode 7 and the magnetic tunnel junction component (MTJ) 8 was carried out on the word line.

[0039] Drawing 76 is the mimetic diagram showing the cross-section structure of the MRAM cel 9. In addition, in drawing 76 , the MRAM cel 9 on a word line 3 is illustrated, a word line 3 is arranged on a silicon substrate 80, on it, the laminating of n+ silicon layer 10 and the p+ silicon layer 11 is carried out, and the pn junction diode 7 is formed. The pn junction diode 7 is covered with the insulator layer of silicon oxide 13 grade.

[0040] And the tungsten stud 12 is arranged in the upper part of the pn junction diode 7, and the pn junction diode 7 is electrically connected to MTJ8 through the tungsten stud 12. In addition, silicon oxide 13 is arranged so that the tungsten stud 12 may also be covered, and flattening of the front face of the tungsten stud 12 and silicon oxide 13 is carried out by CMP (Chemical Mechanical Polishing).

[0041] The template layer 15 (10nm of thickness) which MTJ8 is a laminated structure and consists of platinum (Pt) sequentially from the bottom, The initial ferromagnetic layer 16 (4nm of thickness) which consists of permalloys of nickel81Fe19, It consists of permalloys of the diamagnetic-material layer 18 (10nm of thickness) which consists of Mn54Fe(s)46, CoFe, or nickel81Fe19. It has the ferromagnetic layer 20 (8nm of thickness) to which the magnetization direction was fixed, the tunnel barrier layer 22 which consists of aluminum 2O3, the software ferromagnetic layer 24 which consists of multilayers of CoFe of 2nm of thickness, and nickel81Fe19 of 20nm of thickness, and the contact layer 25 which consists of Pt(s).

[0042] In addition, after depositing aluminum of 1-2nm of thickness, the tunnel barrier layer 22 is processed for 60 - 240 seconds with the power density of 25 W/cm2 under the oxygen pressure force of 100mTorr(s) by the plasma oxidation method, and is formed.

[0043] moreover, small MTJ8 which forms one big MTJ all over the silicon oxide 13 on a substrate 80 in fact, carries out patterning of this by argon ion milling using a photoresist mask, and is shown in drawing 76 although not shown in drawing 76 -- plurality -- forming . Each MTJ8 is covered with silicon oxide 26. Moreover, although not shown in drawing 76 , the contact layer 25 is connected to a bit line.

[0044] The magnetic tunnel resistance of MTJ8 differs by the case where the direction of magnetization of the software ferromagnetic layer 24 is the same as the direction of magnetization of the ferromagnetic layer 20, and the case where the opposite direction is turned to, as explained previously. The direction of magnetization of the software ferromagnetic layer 24 can change a bit line and a word line by the field generated by the flowing current.

[0045] Moreover, the magnetic tunnel resistance of MTJ8 is greatly dependent also on the thickness of the tunnel barrier layer 22 and its barrier height, and the quality-of-the-material property of film, such as roughness of the interface under junction.

[0046] The software ferromagnetic layer 24 is formed so that it may have the easy direction of the magnetization called an easy axis (easy axis). The direction of the magnetization in alignment with this easy axis can turn into a 2-way, and can be made to correspond to two data, 0 and 1, of a memory cell, respectively.

[0047] On the other hand, the ferromagnetic layer 20 is formed so that the direction of magnetization may be the same as the easy axis of the software ferromagnetic layer 24, and may not be based on the operating state of MRAM and a direction may not be changed.

[0048] It is called the direction of fixed magnetization of the direction of this magnetization (expedient translation of unidirectional anisotropy direction). The easy axis of the software ferromagnetic layer 24 is defined combining the intrinsic anisotropy (intrinsic anisotropy) of MTJ8, a stress induction anisotropy (stress induced anisotropy), and the anisotropy resulting from a configuration.
[0049] Here, an intrinsic anisotropy means the anisotropy of the magnetization of physical-properties original which a ferromagnetic has, and a stress induction anisotropy means the anisotropy of the magnetization produced when stress is applied to a ferromagnetic.
[0050] Moreover, as shown in drawing 75 , as for MTJ8, the plane view configuration is carrying out the shape of a rectangle of long side die-length L and shorter side die-length W. This is because the easy axis of the software ferromagnetic layer 24 is defined using the anisotropy resulting from the configuration of MTJ8.
[0051] Next, the setting approach of the direction of fixed magnetization of the ferromagnetic layer 20 is explained. The initial ferromagnetic layer 16 by which deposition formation is carried out on the template layer 15 turns up the field ({111} sides) where crystal orientation turns into {111} bearings, and grows. Moreover, the diamagnetic-material layer 18 which consists of MnFe(s) is deposited on the initial ferromagnetic layer 16.
[0052] These magnetic layers are deposited under the field which was suitable in the same direction as the direction of the easy axis of the software ferromagnetic layer 24 deposited behind, and, thereby, the direction of fixed magnetization of the software ferromagnetic layer 24 is defined.
[0053] Moreover, in order that magnetic flux may close between the ferromagnetic layer 20 and the diamagnetic-material layer 18, in the range of the magnitude of the field generated according to the current which the direction of magnetization of the ferromagnetic layer 20 stops easily being able to change a direction rather than that of the software ferromagnetic layer 24 due to an external magnetic field, and flows a word line and a bit line, the direction of magnetization of the ferromagnetic layer 20 is fixed. Furthermore, since the plane view configuration of MTJ8 is made into the rectangle, the magnetization anisotropy resulting from the configuration of the ferromagnetic layer 20 occurs, and this is also contributing to the stability of the ferromagnetic layer 20 of the direction of magnetization.
[0054] The writing and read-out actuation of MRAM are explained below <the outline of the writing / read-out actuation of MRAM>. If a predetermined current is passed to the word line and bit line (the selection word line and the subdevice-bit line, and name) for performing address selection, a field will occur around each line and the joint field which each field combined will occur in the intersection (selection address) of a both line. If this field is impressed, the direction of magnetization of the software ferromagnetic layer 24 of MTJ8 currently installed in the intersection of a both line will rotate in the field of a layer, and the writing of data will be performed.
[0055] The magnitude of this field is designed so that it may become larger than the switching field (field which the direction of magnetization begins to reverse) of the software ferromagnetic layer 24, and it is mainly decided by the coercive force and the magnetization anisotropy of the software ferromagnetic layer 24.
[0056] Moreover, the field generated around a selection word line and a subdevice-bit line must be designed sufficiently small so that the direction of fixed magnetization of the ferromagnetic layer 20 may not be rotated. Because, it is for not changing the direction of magnetization of a half-selection (Half select) cel. In addition, a half-selection cel is a cel to which the current is flowing to either the word line located up and down or a bit line.
[0057] Thus, in order to reduce the power consumption at the time of writing, the architecture of a memory cell array is designed so that a write-in current may not flow directly to MTJ8.
[0058] Moreover, the data written in the MRAM cel 9 are read by sensing the current which flows the pn junction diode 7 and MTJ8 perpendicularly. In addition, since tunnel current flows the inside of the MRAM cel 9 perpendicularly at the time of actuation, occupancy area of the MRAM cel 9 can be made small.
[0059] Resistance of the tunnel barrier layer 22 which consists of aluminum 2O3 of MTJ8 changes almost exponentially to thickness. That is, the current which flows the tunnel barrier will be reduced if

thickness becomes thick, and only the current which tunnels junction flows perpendicularly to junction.
[0060] And the data of the MRAM cel 9 are read by carrying out the monitor of the electrical potential difference of the MRAM cel 9 generated when a sense current far smaller than a write-in current flows MTJ8 perpendicularly.
[0061] As explained previously, the tunnel probability of MTJ8 increases, so that many density of stateses of the same polar spin as the polarity of the spin in the software ferromagnetic layer 24 in ****** exist in the ferromagnetic layer 20 in a final state.
[0062] Therefore, in both layers, when the same, it is low, and the direction of [when the magnetic tunnel resistance of MTJ8 has the the same condition of the spin of the software ferromagnetic layer 24 and the ferromagnetic layer 20 (i.e., magnetization)] becomes high, when the direction of magnetization is opposite. So, if the monitor of the resistance of MTJ8 is carried out with a minute current, the data of the MRAM cel 9 can be read.
[0063] In addition, the field which a sense current generates can be disregarded and does not affect the condition of magnetization of the MRAM cel 9. Moreover, since wiring required for read-out/writing of the MRAM cel 9 is only the array of the bit line shown in drawing 75 , and a word line, it can constitute an efficient memory cell array.
[0064] Write-in actuation of MRAM is further explained using drawing 77 and drawing 78 below <write-in actuation>.
[0065] Drawing 77 is the representative circuit schematic of the memory cell array shown in drawing 75 , the both ends of word lines 1-3 are connected word line control circuit 53, respectively, and the both ends of bit lines 4-6 are connected to the bit line control circuit 51, respectively. In addition, since facilities are given to explanation of drawing 78 , word lines WL1-WL3 and bit lines 4-6 may be shown for word lines 1-3 as bit lines BL4-BL6.
[0066] And the pn junction diode 7 expressed with MTJ8 expressed with a resistance notation and a diode notation is arranged in the intersection of word lines 1-3 and bit lines 4-6.
[0067] Here, an assumption of the case where a word line 1 and a bit line 4 are chosen chooses MRAM cel 9a located in both intersection.
[0068] Selected MRAM cel cel 9a is written in by the joint field generated according to the current IB which flows a bit line 4, and the current IW which flows a word line 1.
[0069] The field independently generated in a cel field has one smaller than a field required to change the direction of magnetization of software ferromagnetic layer 24 cel of MTJ8 of the currents IB and IW.
[0070] So, writing does not have a line crack in the MRAM cels 9b-9e (cel to which either Current IB or IW flows to a word line and a bit line) which are half-selection cels.
[0071] However, if the field by Currents IB and IW is combined, it will become sufficient magnitude to change the direction of magnetization of the software ferromagnetic layer 24 of selected memory cell 9a.

[0072] In addition, at least one side of Currents IB and IW is designed so that it may flow bidirectionally, so that the magnetization direction of the software ferromagnetic layer 24 of cel 9a may be made in the two opposite different magnetization directions. In addition, in drawing 77 , since the bit line control circuit 51 and the word line control circuit 53 consist of 2 pairs, both currents IB and IW can change the sense of a current.
[0073] Drawing 78 shows the electrical potential difference of bit lines 4-6 (bit lines BL4-BL6) and word lines 1-3 (word lines WL1-WL3), and the timing chart of a current.
[0074] As shown in drawing 78 , the electrical potential difference of the bit lines BL4-BL6 at the time of writing is set as the convenient electrical potential difference Vb, although a current is passed bidirectionally. Moreover, the electrical potential difference of word lines WL1-WL3 is set as the forward electrical potential difference Vw more greatly than an electrical potential difference Vb.
[0075] At the time of standby, these electrical potential differences are set up so that a reverse bias may start the pn junction diode 7 of all the cels 9. Therefore, Currents IB and IW do not flow the inside of a memory cell at the time of standby.

[0076] <Read-out actuation>, next read-out actuation of MRAM are further explained using drawing 77 and drawing 78 . As shown in drawing 78 , the electrical potential difference of a word line WL1 is lowered to Vb from Vw, the electrical potential difference of a bit line BL4 is raised from Vb to Vw, and forward bias is impressed to the pn junction diode 7 of selected cel 9a.
[0077] During read-out, the non-subdevice-bit lines 5 and 6 are still the standby electrical potential differences Vb, and the non-choosing word line 2 and WL 3 is still the standby electrical potential difference Vw.
[0078] In addition, it is that which does not have a voltage drop from a word line to a bit line in the half-selection cels 9b-9e (that is, 0V are impressed to the pn junction diode 7), and a current does not flow the inside of a cel.
[0079] The magnitude of the sense current 30 (refer to drawing 77) which flows from a bit line BL4 to a word line WL1 through cel 9a by the magnetic tunnel resistance of selection cel 9a is determined. In the sense circuit which constitutes a part of bit line control circuit 51, the average of two current values predicted corresponding to two conditions of a cel is made into a reference current, and it compares with a sense current. And the difference of both currents is amplified and the data currently stored in selection cel 9a are read.
[0080] In addition, as shown in the wave of the sense current 30 of drawing 77 , the sense current 30 presents two kinds of current wave forms equivalent to two magnetization conditions of MTJ8.
[0081] After data read-out, although the electrical potential difference of a bit line BL4 and a word line WL1 is returned to each standby value, as for the magnetization condition of memory cell 9a, after read-out actuation is maintained.
[0082]
[Problem(s) to be Solved by the Invention] As explained above, at the time of the writing to a MRAM cel, a current is passed to a bit line and a word line, and a field is generated. And since it was necessary to give a bigger field than the switching field of the software ferromagnetic layer which constitutes a cel to the memory cell of the selection address, the comparatively big current needed to be passed. Therefore, there was a trouble that the power consumption at the time of writing became large.
[0083] It was made in order that this invention might cancel the above troubles, and it sets it as the 1st purpose to offer MRAM which reduced the power consumption at the time of writing.
[0084] Moreover, in the conventional MRAM cel array, it bundled up in the memory-block unit which consists of at least one memory cell array, and there was elimination or a trouble that writing in took time amount, about data.
[0085] This invention sets it as the 2nd purpose to offer MRAM which reduced the time amount spent on elimination and writing.
[0086]
[Means for Solving the Problem] The magnetic storage according to claim 1 concerning this invention Two or more bit line and two or more word lines which cross by non-contact and constitute a matrix, It is arranged by the intersection of said two or more bit lines and said two or more word lines, respectively. It is the magnetic storage equipped with two or more memory cells containing at least one magnetic tunnel junction. Said two or more memory cells It is arranged, respectively between [of said two or more bit lines] 1 and 1 of said two or more word lines. Said at least one magnetic tunnel junction It has the software ferromagnetic layer which can change the direction of magnetization. Said at least one magnetic tunnel junction The easy axis which is the easy direction of magnetization of said software ferromagnetic layer is arranged so that it may have the include angle of 40 - 50 degrees to the extension direction of said two or more bit lines and two or more of said word lines.
[0087] The plane view configuration is constituted by the rectangle so that the magnetic storage according to claim 2 concerning this invention may become longer than the side where said easy axis and the side where said magnetic tunnel junction is parallel to said easy axis cross at right angles.
[0088] The magnetic storage according to claim 3 concerning this invention Two or more bit line and two or more word lines which cross by non-contact and constitute a matrix, It is arranged by the intersection of said two or more bit lines and said two or more word lines, respectively. It is the

magnetic storage equipped with two or more memory cells containing at least one magnetic tunnel junction. It connects with the 1st edge of two or more of said bit lines, respectively. The electric connection between said 1st edge and the 1st power source [2nd] of power-source ****** Two or more 1st switchable change means, It connected with the 2nd edge of two or more of said bit lines, respectively, and has two or more 2nd switchable change means for the electric connection between said 2nd edge and said 1st power source [2nd] of the power-source ****** above.
[0089] The magnetic storage according to claim 4 concerning this invention Each 1st main electrode is connected to the 1st edge of two or more of said bit lines for said 1st change means. Each 2nd main electrode has the 1st and 2nd MOS transistors of the same conductivity type connected to said the 1st power source and said 2nd power source. Said 2nd change means Each 1st main electrode is connected to the 2nd edge of two or more of said bit lines, and each 2nd main electrode has 4 MOS transistors of the 3rd and ** of the same conductivity type connected to said the 1st power source and said 2nd power source.
[0090] The magnetic storage according to claim 5 concerning this invention Each 1st main electrode is connected to the 1st edge of two or more of said bit lines for said 1st change means. Each 2nd main electrode has the 1st and 2nd MOS transistors of differing of the conductivity type connected to said the 1st power source and said 2nd power source. Said 2nd change means Each 1st main electrode is connected to the 2nd edge of two or more of said bit lines, and each 2nd main electrode has the 3rd and 4th MOS transistors from which the conductivity type connected to said the 1st power source and said 2nd power source differs.
[0091] The magnetic storage according to claim 6 concerning this invention Said 1st and 2nd MOS transistors each Said 2nd MOS transistor connected between the main electrodes of the above 1st, and the 5th MOS transistor of the same conductivity type, Said 3rd and 4th MOS transistors each Said 4th MOS transistor connected between the main electrodes of the above 1st, and the 6th MOS transistor of the same conductivity type, It prepares for a pan and the control electrode of said 5th and 6th MOS transistors is connected to the 3rd power source which gives the predetermined electrical potential difference which will always be in an ON state.
[0092] The magnetic storage according to claim 7 concerning this invention Two or more bit line and two or more word lines which cross by non-contact and constitute a matrix, and it being arranged by the intersection of said two or more bit lines and said two or more word lines, respectively, and with two or more memory cells containing at least one magnetic tunnel junction, and two or more memory cell arrays come out of and constituted Had two or more main word lines crossed to said two or more memory cell arrays, and two or more memory cell array selection lines arranged corresponding to each of two or more of said memory cell arrays. It has the memory cell array group of at least 1. Said two or more word lines It connects with the output of the 1st combination logic gate established in the intersection of said two or more main word lines and two or more of said memory cell array selection lines, respectively, respectively. The input of said 1st combination logic gate is connected to 1 of said two or more main word lines in a crossover condition, and 1 of said two or more memory cell array selection lines.
[0093] The magnetic storage according to claim 8 concerning this invention Two or more global word lines which have two or more said memory cell array groups of at least 1, and are crossed to said two or more memory cell array groups, It has further two or more memory cell array group-selection lines arranged corresponding to each of two or more of said memory cell array groups. Said two or more main word lines It connects with the output of the 2nd combination logic gate established in the intersection of said two or more global word lines and two or more of said memory cell array group-selection lines, respectively, respectively. The input of said 2nd combination logic gate is connected to 1 of said two or more global word lines in a crossover condition, and 1 of said two or more memory cell array group-selection lines.
[0094] The magnetic storage according to claim 9 concerning this invention Two or more bit line and two or more word lines which cross by non-contact and constitute a matrix, Two or more memory cell arrays which consist of two or more memory cells which are arranged by the intersection of said two or

more bit lines and said two or more word lines, respectively, and contain at least one magnetic tunnel junction, Had two or more Maine bit lines crossed to said two or more memory cell arrays, and two or more memory cell array selection lines arranged corresponding to each of two or more of said memory cell arrays. It has the memory cell array group of at least 1. Said two or more bit lines It connects with the output of the 1st combination logic gate established in the intersection of said two or more Maine bit lines and two or more of said memory cell array selection lines, respectively, respectively. The input of said 1st combination logic gate is connected to 1 of said two or more Maine bit lines in a crossover condition, and 1 of said two or more memory cell array selection lines.

[0095] The magnetic storage according to claim 10 concerning this invention Two or more global bit lines which have two or more said memory cell array groups of at least 1, and are crossed to said two or more memory cell array groups, It has further two or more memory cell array group-selection lines arranged corresponding to each of two or more of said memory cell array groups. Said two or more Maine bit lines It connects with the output of the 2nd combination logic gate established in the intersection of said two or more global bit lines and two or more of said memory cell array group-selection lines, respectively, respectively. The input of said 2nd combination logic gate is connected to 1 of said two or more global bit lines in a crossover condition, and 1 of said two or more memory cell array group-selection lines.

[0096] The magnetic storage according to claim 11 concerning this invention Two or more bit line and two or more word lines which cross by non-contact and constitute a matrix, And the memory cell array which consists of two or more memory cells which are arranged by the intersection of said two or more bit lines and said two or more word lines, respectively, and contain at least one magnetic tunnel junction, It has an inductor, said at least one magnetic tunnel junction has the software ferromagnetic layer which can change the direction of magnetization, and said inductor generates a field in the direction in alignment with the easy axis which is the easy direction of magnetization of said software ferromagnetic layer.

[0097] Said at least one magnetic tunnel junction is arranged so that, as for the magnetic storage according to claim 12 concerning this invention, said easy axis may agree in the extension direction of said two or more bit lines or two or more of said word lines, and it is the coiled form inductor arranged so that said inductors might surround said memory cell array along the extension direction of said two or more bit lines or said two or more word lines which agree with the direction of said easy axis.

[0098] The magnetic storage according to claim 13 concerning this invention Two or more bit line and two or more word lines which cross by non-contact and constitute a matrix, And at least one memory cell array which consists of two or more memory cells which are arranged by the intersection of said two or more bit lines and said two or more word lines, respectively, and contain at least one magnetic tunnel junction, It is prepared in the outside of said two or more bit lines and said two or more word lines of said at least one memory cell array, respectively. It has at least one wrap plate-like flash plate bit line and at least one flash plate word line for the formation field of said two or more bit lines and two or more of said word lines.

[0099] The magnetic storage according to claim 14 concerning this invention has two or more said at least one memory cell arrays, said two or more memory cell arrays are arranged in the shape of a matrix, and in accordance with the array of two or more of said memory cell arrays, two or more arrangement of said at least one flash plate bit line and at least one flash plate word line is carried out, respectively so that a matrix may be constituted.

[0100] The magnetic storage according to claim 15 concerning this invention Two or more bit line and two or more word lines which cross by non-contact and constitute a matrix, And the memory cell array which consists of two or more memory cells which are arranged by the intersection of said two or more bit lines and said two or more word lines, respectively, and contain at least one magnetic tunnel junction, Even if there are few said two or more bit lines and two or more word lines, it is arranged in two edges of the method of one, respectively. It has at least one inductor which saves the current of the selected bit line and a word line which flows to the method of one at least by LC resonance, and at least one capacitor.

[0101] The magnetic storage according to claim 16 concerning this invention It has two or more said at least one inductors and said at least one capacitors. Said two or more bit lines Two become a pair and two or more bit line pairs are constituted. Said two or more inductors Corresponding to said two or more each of a bit line pair, two or more 1st inductors arranged so that it might connect electrically between bit lines are included. Said two or more capacitors In the edge opposite to the arrangement side of two or more of said inductors, two or more 1st capacitors electrically connected corresponding to each of two or more of said bit lines are included.
[0102] The magnetic storage according to claim 17 concerning this invention Two become a pair and said two or more word lines constitute two or more WORD line pairs. Said two or more inductors Corresponding to each of two or more of said WORD line pairs, two or more 2nd inductors arranged so that it might connect electrically between word lines are included further. Said two or more capacitors In the edge opposite to the arrangement side of two or more of said inductors, two or more 2nd capacitors electrically connected corresponding to each of two or more of said word lines are included further.
[0103] The magnetic storage according to claim 18 concerning this invention At least one semiconductor chip and the screen which consists of conductors and contains said at least one semiconductor chip, The package which consists of resin and contains said screen, and the base substrate which closes and seals opening of said package, With the bump for signal transmissions who is arranged in the outside principal plane of said base substrate, and performs the signal transmission of said at least one semiconductor chip and exterior It is arranged so that said bump for signal transmissions may be surrounded, and it has the bump for electric shielding electrically connected to said screen. Said at least one semiconductor chip The magnetic storage chip equipped with the memory cell array constituted by having two or more memory cells containing at least one magnetic tunnel junction is included.
[0104] The magnetic storage according to claim 19 concerning this invention is further equipped with the 1st stress relaxation film arranged in the inside and the outside of the opening edge of said screen, and the 2nd stress relaxation film arranged by the wall of said screen.
[0105] Including further the circuit chip in which, as for the magnetic storage according to claim 20 concerning this invention, said at least one semiconductor chip includes the circumference circuit of said memory cell array, said account chip of the MAG and said circuit chip are piled up up and down, and are contained by said electric shielding inside of the body.
[0106] The magnetic storage according to claim 21 concerning this invention has the software ferromagnetic layer in which at least one magnetic tunnel junction can change the direction of magnetization, and said screen consists of ferromagnetics which have said software ferromagnetic layer and EQC, and bigger permeability than it.
[0107] As for the magnetic storage according to claim 22 concerning this invention, said screen consists of the antiferromagnetic substance.
[0108] As for the magnetic storage according to claim 23 concerning this invention, said screen consists of multilayers of a ferromagnetic and the antiferromagnetic substance.
[0109] The magnetic-substance substrate according to claim 24 concerning this invention has at least the multilayers which form at least one magnetic tunnel junction arranged throughout the principal plane.
[0110] The magnetic-substance substrate according to claim 25 concerning this invention contains the diamagnetic-material layer in which said multilayers were arranged in order as said at least one magnetic tunnel junction, the ferromagnetic layer, the tunnel barrier layer which consists of insulators, and the software ferromagnetic layer.
[0111] The two-layer film of the 1st conductivity-type impurity layer and the 2nd conductivity-type impurity layer from which said multilayers are arranged by the lower part of said at least one magnetic tunnel junction, and the magnetic-substance substrate according to claim 26 concerning this invention constitutes pn junction is included further.
[0112] The magnetic-substance substrate according to claim 27 concerning this invention has said multilayers on the SOI substrate equipped with the substrate section used as a foundation, and the SOI layer which was arranged on this substrate section and which embedded and was arranged on the oxide

film and this embedding oxide film.
[0113]
[Embodiment of the Invention] MRAM concerning the gestalt 1 of operation of <gestalt 1 of A. operation> <description of gestalt of this operation> this invention is characterized by the easy axis of the software ferromagnetic layer which constitutes a MRAM cel not being parallel to a bit line and a word line, and arranging a MRAM cel so that a bit line and a word line, and the include angle of 40 - 50 degrees may more specifically be made.
[0114] <an A-1. equipment configuration <the configuration of an A-1-1.MRAM cel>> -- the typical configuration of a MRAM cel is first explained using drawing 1 . The MRAM cel MC shown in drawing 1 has the pn junction diode 7 with which the laminating of n+ silicon layer 10 and the p+ silicon layer 11 is carried out, and they are constituted.
[0115] And the tungsten stud 12 is arranged in the upper part of the pn junction diode 7, and the pn junction diode 7 is electrically connected to the magnetic tunnel junction (Magnetic Tunnel Junction:MTJ) 8 through the tungsten stud 12.
[0116] The template layer 15 (10nm of thickness) which MTJ8 is a laminated structure and consists of platinum (Pt) sequentially from the bottom, The initial ferromagnetic layer 16 (4nm of thickness) which consists of permalloys of nickel81Fe19, It consists of permalloys of the diamagnetic-material layer 18 (10nm of thickness) which consists of Mn54Fe(s)46, CoFe, or nickel81Fe19. It has the ferromagnetic layer 20 (8nm of thickness) to which the magnetization direction was fixed, the tunnel barrier layer 22 which consists of aluminum 2O3, the software ferromagnetic layer 24 which consists of multilayers of CoFe of 2nm of thickness, and nickel81Fe19 of 20nm of thickness, and the contact layer 25 which consists of Pt(s).
[0117] The plane view configuration of the MRAM cel MC is a rectangle, and they are set up so that a direction parallel to the long side may serve as an easy axis in the direction of the spin of the electron of the software ferromagnetic layer 24. [including MTJ8] In addition, a direction parallel to a shorter side serves as a hard axis (hard axis) which is the difficult direction of magnetization.
[0118] The flat-surface configuration of the conventional MRAM cel array is shown in <examination with detailed MRAM cel array of the A-1-2. former> drawing 2 . In addition, the MRAM cel MC 1 is shown as a perspective view for convenience.
[0119] As shown in drawing 2 , two or more bit lines BL1 arranged in parallel mutually are arranged so that it may cross in the upper part of two or more word lines WL1 arranged in parallel mutually.
[0120] And the MRAM cel (only calling a cel henceforth) MC 1 is formed in each intersection across which it faces with a word line and a bit line. In addition, the arrow head shown typically shows the direction of the spin of the software ferromagnetic layer 24 of the MRAM cel MC 1 to each MRAM cel MC 1, and the spin direction of all the MRAM cels MC 1 has become rightward in the state of the standby shown in drawing 2 . In addition, although [the configuration of the MRAM cel MC 1] it is the same as that of the memory cell MC shown in drawing 1 , it is not necessarily limited to this configuration.
[0121] Drawing 3 is the top view showing the condition of writing typically in the conventional MRAM cel array. In addition, the sign of MC1a, MC1b, and MC1c may be attached and distinguished for convenience in the MRAM cel MC 1 below.
[0122] If a predetermined current is passed to the word line and bit line (the selection word line and the subdevice-bit line, and name) for performing address selection at the time of writing, around a current, a field will occur with the principle of BIO savart (Biot-Savart).
[0123] Here, the field which generates the field generated around a bit line around Hx and a word line is set to Hy. And a selection word line and a subdevice-bit line are written as WL1a and BL1a for convenience, respectively.
[0124] In addition, the direction where the current in drawing 3 flows is the right from the left in selection word line WL1a upwards in subdevice-bit line BL1b from the bottom.
[0125] If a predetermined current is passed to selection word line WL1a and subdevice-bit line BL1b, in the intersection (selection address) of a both line, Fields Hx and Hy will join together. If this joint field

is impressed, the direction of magnetization of the software ferromagnetic layer 24 of MRAM cel MC1a currently installed in the intersection of selection word line WL1a and subdevice-bit line BL1b will rotate in the field of a layer, and the writing of data will be performed. In drawing 3 , the spin direction of MRAM cel MC1a rotates 90 degrees or more, and is shown.
[0126] And by the magnetization anisotropy by the cel configuration, since spin rotates to the direction of an easy axis, finally spin will be reversed (180-degree rotation).
[0127] Also in two or more MRAM cel MC1b shown in the MRAM cel which is half-selection (half-select) 9 cel to which the current is flowing to either the word line located up and down or a bit line, i.e., drawing 3 , on the other hand, although the spin of the software ferromagnetic layer 24 rotates, each current is set to reversal so that it may not result.
[0128] In addition, since the field Hx of two or more half-selection cel MC1c depended on subdevice-bit line BL1a generated around subdevice-bit line BL1a is the same as that of the direction of an easy axis, the big rotation like [it displays on drawing 3] cannot be caused only by Field Hx.
[0129] The relation of the three above-mentioned field in the case of forming the field Hk required for making drawing 4 reverse spin by the joint field with Fields Hx and Hy is shown. In drawing 4 , Field Hk is shown on an axis of abscissa, and Field Hy is shown on the axis of ordinate. Moreover, the relation concerned is expressed with a formula below.
[0130]
[Equation 3]

$$H_x^{2/3} + H_y^{2/3} = H_k^{2/3} \quad \cdots (3)$$

[0131] The curve in drawing 4 is called an asteroid curve. And when Field Hk is expressed with the following formula (4), the spin of the software ferromagnetic layer 24 is reversed.
[0132]
[Equation 4]

$$H_x^{2/3} + H_y^{2/3} > H_k^{2/3} \quad \cdots (4)$$

[0133] Moreover, when Field Hk is expressed with the following formula (5), the direction of the spin of the software ferromagnetic layer 24 is maintained.
[0134]
[Equation 5]

$$H_x^{2/3} + H_y^{2/3} < H_k^{2/3} \quad \cdots (5)$$

[0135] The flux density B generated around the stationary current I is expressed with a formula (6) below from Biot-Savart law.
[0136]
[Equation 6]

$$B(R) = \frac{\mu}{2\pi} \cdot \frac{I}{R} \quad \cdots (6)$$

[0137] Here, mu is permeability and R is the distance from Current I. Moreover, Field H and flux density B have the relation expressed with a formula (7) below.
[0138]
[Equation 7]

$$B = \mu H \quad \cdots (7)$$

[0139] Therefore, the following formulas (8) are realized.
[0140]
[Equation 8]

$$H(R) = \frac{1}{2\pi} \cdot \frac{I}{R} \quad \cdots (8)$$

[0141] The above-mentioned formula (8) shows that Field H is proportional to the stationary current I. Therefore, in order to lower the power consumption at the time of writing, it is desirable to lower the field Hk required to reverse spin, i.e., to make Hx+Hy as small as possible.
[0142] Artificers reached the configuration of the MRAM cel array which can reduce Field Hk based on examination of the conventional technique mentioned above.
[0143] The flat-surface configuration of the MRAM cel array MA 10 which starts the gestalt 1 of operation of this invention at the configuration of an A-1-3.MRAM cel array and drawing 5 <of operation> is shown. As shown in drawing 5 , two or more bit lines BL1 arranged in parallel mutually are arranged so that it may cross in the upper part of two or more word lines WL1 arranged in parallel mutually.
[0144] And the MRAM cel MC 2 is formed in each intersection across which it faces with a word line and a bit line. In addition, although [the configuration of the MRAM cel MC 2] it is the same as that of the memory cell MC shown in drawing 1 , it is not necessarily limited to this configuration.
[0145] As shown in drawing 5 , each MRAM cel MC 3 is arranged so that an easy axis may incline 45 degrees to a bit line and a word line. In addition, in this example, since it leans to the diagonal right 45 degrees and is arranged in it to the word line WL1, in the state of the standby shown in drawing 5 , the spin direction of all the MRAM cels MC 2 has diagonally right sense.
[0146] Drawing 6 is the top view showing typically the condition of the writing of the MRAM cel array MA 10. In addition, the sign of MC2a, MC2b, and MC2c may be attached and distinguished for convenience in the MRAM cel MC 2 below.
[0147] If a predetermined current is passed to selection word line WL1a and subdevice-bit line BL1b, in the intersection (selection address) of a both line, Fields Hx and Hy will join together. In addition, the direction where the current in drawing 6 R> 6 flows is the right from the left in selection word line WL1a upwards in subdevice-bit line BL1b from the bottom.
[0148] If this joint field is impressed, the direction of magnetization of the software ferromagnetic layer 24 of MRAM cel MC1a currently installed in the intersection of selection word line WL1a and subdevice-bit line BL1b will rotate in the field of a layer, and the writing of data will be performed. In drawing 6 , the spin direction of MRAM cel MC2a rotates 90 degrees or more, and is shown.
[0149] And by the magnetization anisotropy by the cel configuration, since spin rotates to the direction of an easy axis, finally spin will be reversed (180-degree rotation).
[0150] Also in two or more MRAM cel MC2bs shown in the MRAM cel which is a half-selection cel to which the current is flowing to either the word line located up and down or a bit line, i.e., drawing 6 , on the other hand, and MC2c, although the spin of the software ferromagnetic layer 24 rotates, each current is set to reversal so that it may not result.
[0151] Although the spin of the software ferromagnetic layer 24 rotates two or more half-selection cel MC2c depended on subdevice-bit line BL1a here so that it may display on drawing 6 since the field Hx generated around subdevice-bit line BL1a crosses at the include angle of about 45 degrees to the direction of an easy axis Spin can also be reversed by adjusting the magnitude of each current, and it cannot be made reversed, either. This is the same also about two or more half-selection cel MC2bs depended on selection word line WL1a.
[0152] The flat-surface configuration of the MRAM cel array MA 20 is shown in <example of configuration of A-1-4. and others> drawing 7 as an example of a configuration of others of the gestalt 1 of operation. As shown in drawing 7 , two or more bit lines BL1 arranged in parallel mutually are arranged so that it may cross in the upper part of two or more word lines WL1 arranged in parallel mutually.
[0153] And the MRAM cel MC 3 is formed in each intersection across which it faces with a word line and a bit line. In addition, although [the configuration of the MRAM cel MC 3] it is the same as that of the memory cell MC shown in drawing 1 , it is not necessarily limited to this configuration.
[0154] As shown in drawing 7 , each MRAM cel MC 3 is arranged so that an easy axis may incline 45 degrees to a bit line and a word line. In addition, in this example, since it leans to the diagonal below 45

degrees and is arranged in it to the word line WL1, in the state of the standby shown in drawing 7 , the spin direction of all the MRAM cels MC 3 has diagonally right sense.
[0155] Drawing 8 is the top view showing typically the condition of the writing of the MRAM cel array MA 20. In addition, the sign of MC3a, MC3b, and MC3c may be attached and distinguished for convenience in the MRAM cel MC 3 below.
[0156] If a predetermined current is passed to selection word line WL1a and subdevice-bit line BL1a, in the intersection (selection address) of a both line, Fields Hx and Hy will join together.
[0157] In addition, the direction where the current in drawing 8 flows is the right from the left in selection word line WL1a upwards in subdevice-bit line BL1a from the bottom.
[0158] If this joint field is impressed, the direction of magnetization of the software ferromagnetic layer 24 of MRAM cel MC3a currently installed in the intersection of selection word line WL1a and subdevice-bit line BL1a will rotate in the field of a layer, and the writing of data will be performed. In drawing 8 , the spin direction of MRAM cel MC3a rotates 90 degrees or more, and is shown.
[0159] And by the magnetization anisotropy by the cel configuration, since spin rotates to the direction of an easy axis, finally spin will be reversed (180-degree rotation).
[0160] On the other hand, although the spin of the software ferromagnetic layer 24 rotates also in two or more MRAM cel MC2bs and MC2c which are the half-selection cel shown in drawing 8 , each current is set to reversal so that it may not result.
[0161] Optimization of the arrangement direction of a MRAM cel is explained using <optimization of the arrangement direction of an A-1-5.MRAM cel> next drawing 9 - drawing 25 .
[0162] First, the case where the direction of spin is reversed by the joint field Hk is explained.
[0163] The relation of the direction of the spin of MRAM cel MC1a of the selection address at the time of the writing in the conventional MRAM cel array shown in drawing 9 and drawing 10 at drawing 2 and the direction of the joint field Hk which reverses it is shown typically.
[0164] In drawing 9 and drawing 10 , if the case where the magnitude of Fields Hx and Hy is the same is assumed, spin and the include angle which the joint field Hk makes will turn into theta1=135 degree.
[0165] Moreover, the relation of the direction of the spin of MRAM cel MC2a of the selection address at the time of the writing in the MRAM cel array MA 10 shown in drawing 11 and drawing 12 at drawing 5 and the direction of the joint field Hk which reverses it is shown typically.
[0166] In drawing 11 and drawing 12 , if the case where the magnitude of Fields Hx and Hy is the same is assumed, spin and the include angle which the joint field Hk makes will turn into theta2=90 degree.
[0167] Moreover, the relation of the direction of the spin of MRAM cel MC3a of the selection address at the time of the writing in the MRAM cel array MA 20 shown in drawing 13 and drawing 14 at drawing 7 and the direction of the joint field Hk which reverses it is shown typically.
[0168] In drawing 13 and drawing 14 , if the case where the magnitude of Fields Hx and Hy is the same is assumed, spin and the include angle which the joint field Hk makes will turn into theta3=180 degree.
[0169] Next, the relation between the joint field Hk and Fields Hx and Hy is shown in drawing 15 . although this relation is the same as what was shown as an asteroid curve in drawing 4 -- |Hx|+|Hy|= -- under the conditions, i.e., the condition of a write-in fixed current, of being fixed, if the fields Hx and Hy on an asteroid curve are searched for, Hx=Hy=Hk / relation of 2root2 will be obtained.
[0170] If based on this, in the conventional MRAM cel array shown in drawing 9 and drawing 10 , spin will be rotated about 135 degrees by the joint field Hk, and 180 degrees will rotate spin from there using the magnetization anisotropy by the configuration.
[0171] On the other hand, in the MRAM cel array MA 10 shown in drawing 11 and drawing 12 , spin rotates about 90 degrees in the magnitude of the same joint field. Therefore, even if it uses the magnetization anisotropy by the configuration, it is [whether spin is reversed and] in a critical condition. So, when taking the configuration of the MRAM cel array MA 10, it is desirable to enlarge Field Hx a little rather than Field Hy, and to make the angle of rotation theta 2 of spin into 90 degrees or more.
[0172] In addition, in the MRAM cel array MA 20 shown in drawing 13 and drawing 14 , since spin rotates about 180 degrees in the magnitude of the same joint field, spin can be reversed certainly.

[0173] Next, even if the joint field Hk is added, the relation of the direction of spin and the direction of the joint field Hk which maintains it is typically shown in drawing 16 - drawing 21 about the case where the direction of spin is maintained. In addition, since drawing 16 - drawing 21 support drawing 9 - drawing 14 , the overlapping explanation is omitted.
[0174] In drawing 16 and drawing 17 , if the case where the magnitude of Fields Hx and Hy is the same is assumed, spin and the include angle which the joint field Hk makes will turn into theta11=45 degree.
[0175] In drawing 18 and drawing 19 , if the case where the magnitude of Fields Hx and Hy is the same is assumed, spin and the include angle which the joint field Hk makes will turn into theta12=0 degree.
[0176] In drawing 20 and drawing 21 , if the case where the magnitude of Fields Hx and Hy is the same is assumed, spin and the include angle which the joint field Hk makes will turn into theta13=90 degree.
[0177] Therefore, in the conventional MRAM cel array shown in drawing 16 , in the MRAM cel array MA 10 which the direction of spin is mostly maintained and is shown in drawing 18 , although writing is performed so that it may be maintained completely, in the MRAM cel array MA 20 shown in drawing 20 , the direction of spin is [whether spin is reversed and] in a critical condition, and is not desirable.
[0178] It is desirable to take into consideration the sense of the current which adopts the configuration of the MRAM cel array MA 20 shown in drawing 13 and drawing 20 , and is passed to a bit line and a word line from the above consideration. The configuration concerned is explained using drawing 22 - drawing 25 .
[0179] In the configuration of the MRAM cel array MA 20, as for drawing 22 and drawing 23 , the direction where a current flows like drawing 8 shows typically the relation of the direction of the joint field Hk which reverses the direction of the spin of MRAM cel MC3a of the selection address at the time of the writing in the case of being the right from the left in selection word line WL1a, and it from the bottom upwards to in subdevice-bit line BL1a.
[0180] In drawing 22 and drawing 23 , if the case where the magnitude of Fields Hx and Hy is the same is assumed, spin and the include angle which the joint field Hk makes turn into theta4=180 degree, and it can be said that it is the configuration that it was suitable when data were written in by reversing the direction of spin.
[0181] Moreover, drawing 24 and drawing 25 show typically the relation of the direction of the spin of MRAM cel MC3a of the selection address at the time of writing when the direction where a current flows has turned on the left from the right in selection word line WL1a down in subdevice-bit line BL1a from the top, and the direction of the joint field Hk which maintains it in the configuration of the MRAM cel array MA 20.
[0182] In addition, compared with the case of drawing 22 , the sense of the current passed to a bit line and a word line is changed.
[0183] In drawing 24 and drawing 25 , if the case where the magnitude of Fields Hx and Hy is the same is assumed, spin and the include angle which the joint field Hk makes turn into theta5=0 degree, and it can be said that it is the configuration that it was suitable when data were written in by maintaining the direction of spin.
[0184] Moreover, also in which configuration of drawing 22 and drawing 24 , since the direction and easy axis of a joint field are in agreement, it has further the advantage that the error of writing becomes smaller than before.
[0185] As explained beyond the <A-2. operation effectiveness>, according to MRAM of the gestalt 1 of operation concerning this invention It is leaning and arranging the easy axis of the software ferromagnetic layer 24 which constitutes a MRAM cel so that the include angle of 45 degrees may be aslant made desirably 40 to 50 degrees to a bit line and a word line. With few write-in currents, the direction of the spin of the MRAM cel in the selection address can be reversed certainly, and the power consumption at the time of writing can be reduced.
[0186] Moreover, by changing the sense of the current passed to a bit line and a word line by the case where the direction of the spin of the MRAM cel in the selection address is reversed, and the case where the direction of spin is maintained, the direction and easy axis of a joint field are made in agreement, and the error of writing can also be reduced.

[0187] MRAM concerning the gestalt 2 of operation of <gestalt 2 of B. operation> <description of gestalt of this operation> this invention The both ends of the bit line of a MRAM cel array and a word line are equipped with read-out / write-in control circuit of a pair. As a configuration of the circuit concerned The 1st MOS transistor which connects a bit line and supply voltage VDD, It has the function to write in both directions of a bit line at the time of writing, and to pour an electric wire, and the function which outputs the electrical potential difference which originates in a sense current at the time of read-out to a sense amplifier including the 2nd transistor which connects a bit line and the touch-down electrical potential difference VSS.
[0188] <B-1. equipment configuration <whole B-1-1.MRAM configuration>> drawing 26 is the block diagram showing the configuration of MRAM concerning the gestalt 2 of operation of this invention, and shows the MRAM cel array MCA and its circumference circuit.
[0189] drawing 26 -- setting -- the train address buffer (column address buffer) CAB -- a train address signal -- receiving -- a signal -- reversal -- or it amplifies and outputs to the train decoder CD.
[0190] The train decoder CD decodes a train address signal, and outputs the decoded signal to Multiplexer MUX.
[0191] Multiplexer MUX chooses a bit line according to the decoded train address signal. A signal is outputted to coincidence in the 1st control circuit CRW1 of train read-out / writing of a bit line connected to an edge on the other hand, and it reads from the 1st control circuit CRW1 of train read-out / writing, or an electrical potential difference and a current are impressed to a subdevice-bit line according to writing.
[0192] the line address buffer (row address buffer) RAB -- a line address signal -- receiving -- a signal -- reversal -- or it amplifies and outputs to the line decoder RD.
[0193] The line decoder RD decodes a line address signal, and chooses a word line according to the decoded line address signal. A signal is outputted to coincidence in the 1st control circuit RRW1 of line read-out / writing of a bit line connected to an edge on the other hand, and it reads from the 1st control circuit RRW1 of line read-out / writing, or an electrical potential difference and a current are impressed to a selection word line according to writing.
[0194] Moreover, as for the data read from the MRAM cel array MCA, or the data written in the MRAM cel array MCA, I/O of data is performed between the exteriors through an input output buffer IOB.
[0195] In addition, the 2nd control circuit CRW2 of train read-out / writing is connected to the another side edge of a bit line, and the 2nd control circuit RRW2 of line read-out / writing is connected to the another side edge of a word line.
[0196] <Detail configuration of B-1-2.MRAM> drawing 27 R> 7 shows the circuit diagram about the configuration except Multiplexer MUX, the train decoder CD, the line decoder RD, and an input output buffer IOB among MRAM(s) shown in drawing 26 . Moreover, about the train address buffer CAB and the line address buffer RAB, illustration is omitted for convenience. In addition, MRAM of a configuration of being shown in drawing 27 calls MRAM100.
[0197] In drawing 27 , the MRAM cel array MCA has the MRAM cels MC11, MC21, MC12, and MC22. A magnetic tunnel junction (MTJ) and pn junction diode have the structure connected to the serial, any MRAM cel expresses MTJ with variable resistance in drawing 27 , and the series connection circuit with diode is expressed as an equal circuit.
[0198] MTJ is expressed with variable resistance in the software ferromagnetic layer (the modification possibility of, i.e., modification of the direction of magnetization, is possible for the direction of an electron spin) which constitutes MTJ, and a ferromagnetic layer (the direction of immobilization, i.e., magnetization, is fixed by the direction of an electron spin), because tunnel resistance becomes small when both spin has turned to the same direction, and tunnel resistance becomes large when having turned to the opposite direction mutually. Therefore, this variable resistance will have two resistance.
[0199] The MRAM cel MC 11 has the variable resistance R11 and diode D11 by which series connection was carried out between the bit line BL1 and the word line WL1. The MRAM cel MC 21 It has the variable resistance R21 and diode D21 by which series connection was carried out between the

bit line BL1 and the word line WL2. The MRAM cel MC 12 Having the variable resistance R12 and diode D12 by which series connection was carried out between the bit line BL2 and the word line WL1, the MRAM cel MC 22 has the variable resistance R22 and diode D22 by which series connection was carried out between the bit line BL2 and the word line WL2.

[0200] Bit lines BL1 and BL2 have the composition that the drain electrical potential difference VDD is given through the NMOS transistors MN11 and MN21, respectively, in the 2nd control circuit CRW2 of train read-out / writing. And the drain electrode of the NMOS transistors MN12 and MN22 is connected to the drain electrode of the NMOS transistors MN11 and MN21, respectively, and it has become the source electrode of the NMOS transistors MN12 and MN22 with the configuration that the source electrical potential difference VSS is given.

[0201] Moreover, the output of NAND gates ND1, ND2, ND3, and ND4 is given to the gate electrode of the NMOS transistors MN11, MN12, MN21, and MN22, respectively, and each input which is three of NAND gates ND1-ND4 is connected to Multiplexer MUX.

[0202] Bit lines BL1 and BL2 have the composition that the drain electrical potential difference VDD is given through the NMOS transistor MN13, variable resistance R31 and MN23, and variable resistance R32, respectively, in the 1st control circuit CRW1 of train read-out / writing. And the drain electrode of the NMOS transistors MN14 and MN24 is connected to the drain electrode of the NMOS transistors MN13 and MN23, respectively, and it has become the source electrode of the NMOS transistors MN14 and MN24 with the configuration that the source electrical potential difference VSS is given.

[0203] In addition, the source electrode of the NMOS transistors MN13 and MN23 is connected also to the multiplexer MUX containing a sense amplifier for detection of a sense current.

[0204] Moreover, the output of NAND gates ND5, ND6, ND7, and ND8 is given to the gate electrode of the NMOS transistors MN13, MN14, MN23, and MN24, respectively, and each input which is three of NAND gates ND1-ND4 is connected to Multiplexer MUX.

[0205] Word lines WL1 and WL2 have the composition that the drain electrical potential difference VDD is given through the NMOS transistors QN11 and QN21, respectively, in the 1st control circuit RRW1 of line read-out / writing. And the drain electrode of the NMOS transistors QN12 and QN22 is connected to the drain electrode of the NMOS transistors QN11 and QN21, respectively, and it has become the source electrode of the NMOS transistors QN12 and QN22 with the configuration that the source electrical potential difference VSS is given.

[0206] Moreover, the gate electrode of the NMOS transistors QN11, QN12, QN21, and QN22 is connected to the line decoder RD.

[0207] Word lines WL1 and WL2 have the composition that the source electrical potential difference VSS is given through the NMOS transistors QN13 and QN14, respectively, in the 2nd control circuit RRW2 of line read-out / writing.

[0208] In addition, in drawing 27 , although the MRAM cel array MCA is made into the cel array of two-line two trains, the size of a row and column is not limited to this.

[0209] Actuation of MRAM100 is explained using drawing 27 - drawing 29 R> 9 below <B-2. equipment actuation>. Drawing 2828 is the timing chart of the various currents in MRAM100 at the time of read-out and writing, and an electrical potential difference.

[0210] While the timing chart of the electrical potential difference given to the word line and bit line for writing and read-out of the timing chart of a sense current and the MRAM cels MC11, MC21, and MC12 in drawing 28 is shown The timing chart of the gate voltage V11, V12, V13, and V14 given to each gate electrode of the NMOS transistors MN11, MN12, MN13, and MN14, The timing chart of the gate voltage VW1, VW2, and VW3 given to the gate electrode of the NMOS transistors QN11, QN12, and QN13 and the timing chart of the source electrical potential difference VS 1 of the NMOS transistor MN13 are shown.

[0211] Moreover, in drawing 28 , the electrical potential differences at the time of standby of a word line and a bit line are electrical potential differences VW and Vb.

[0212] Since pn junction diode is contained in each MRAM cel, electrical potential differences VW and Vb are impressed to a word line and a bit line so that a reverse bias may be impressed to the pn junction

of the diode concerned at the time of standby. In addition, since each diode is constituted so that a cathode may be connected to a word line as shown in drawing 27 , it is set up so that it may become the relation of VW>Vb.

[0213] It is assumed to below as the electrical-potential-difference Vb= source electrical potential difference VSS, and control of a bit line BL1 is explained to it.

[0214] As shown in <B-2-1. standby condition> drawing 28 , in the state of standby, as for all word lines, an electrical potential difference VW is impressed, and, as for all bit lines, an electrical potential difference Vb is impressed. In order to realize this, four NMOS transistors MN11, MN12, MN13, and MN14 shown in drawing 28 are arranged.

[0215] That is, the source electrical potential difference VSS is given to gate voltage V11 and V13 so that the NMOS transistors MN11 and MN13 may be in an OFF state at the time of standby, and the drain electrical potential difference VDD is given to gate voltage V12 and V14 so that the NMOS transistors MN12 and MN14 may be in an ON state.

[0216] Moreover, gate voltage VW1 is impressed so that the NMOS transistor QN11 may be in an ON state, gate voltage VW2 is impressed so that the NMOS transistor QN12 may be in an OFF state, and gate voltage VW3 is impressed so that the NMOS transistor QN13 may be in an OFF state.

[0217] In addition, since the source electrode is connected to the drain electrical potential difference VDD, the NMOS transistor QN11 impresses the electrical potential difference of VDD+delta VDD as gate voltage VW1. This is for compensating the voltage drop by the threshold electrical potential difference of a transistor.

[0218] Consequently, the source electrical potential difference VSS is given to a bit line BL1, and the drain electrical potential difference VDD is given to a word line WL1.

[0219] When writing data "1" in the <B-2-2. write-in condition 1 (Wright 1)> MRAM cel MC 11 (the direction of spin is reversed), it is necessary to pass a current on the selection word line WL1 and the subdevice-bit line BL1. In MRAM100 shown in drawing 27 R> 7, it assumes that a current flows bidirectionally only to a bit line.

[0220] In this case, make the NMOS transistors MN11 and MN14 into an ON state, and let the NMOS transistors MN12 and MN13 be OFF states. However, since the source electrode is connected to the drain electrical potential difference VDD, the NMOS transistor MN11 impresses the electrical potential difference of VDD+delta VDD as gate voltage V11.

[0221] Consequently, the current IBT which flows a bit line BL1 will flow toward the bottom from on drawing 27 .

[0222] To the selection word line WL1, Current IWD will flow toward the right from the left of drawing 27 by making the NMOS transistors QN11 and QN13 into an ON state, and on the other hand, making the NMOS transistor QN12 into an OFF state. Since the source electrode is connected to the drain electrical potential difference VDD, the NMOS transistor QN11 impresses the electrical potential difference of VDD+delta VDD as gate voltage Vw1.

[0223] Thus, the spin of the software ferromagnetic layer of MTJ of the MRAM cel MC 11 rotates the selection word line WL1 and the subdevice-bit line BL1 by the field resulting from the flowing currents IWD and IBT, and data are written in.

[0224] When reading the data "1" written in the <B-2-3. read-out condition 1 (lead 1)> MRAM cel MC 11, forward bias is impressed only to the diode D11 of the MRAM cel MC 11, and the sense current ISC is passed. If this sense current ISC flows the MRAM cel MC 11, a bit line BL1 will cause a voltage drop. Data judge "0" and "1" in the magnitude of this voltage drop.

[0225] In order to impress forward bias to diode D11, an electrical potential difference Vb is impressed to the selection word line WL1, and an electrical potential difference Vw is impressed to the subdevice-bit line BL1. In order to realize this condition, make the NMOS transistors MN11 and MN13 into an ON state, and let the NMOS transistors MN12 and MN14 be OFF states.

[0226] However, since the source line of the NMOS transistors MN11 and MN13 is VDD, the electrical potential difference of VDD+delta VDD is impressed as gate voltage V11 and V13.

[0227] At this time, a reverse bias (it is an electrical potential difference Vb to an electrical potential

difference VW and a bit line BL2 in a word line WL2) is impressed to the pn junction diode D22 of the MRAM cel MC 22 of the non-choosing address, the potential difference is not given to the diodes D12 and D21 of the MRAM cels MC12 and MC21 of the half-selection address (0 bias), and a current does not flow in the MRAM cels MC12, MC21, and MC22.
[0228] Here, RH and the value of the lower one are set to RL for the value of the higher one between two resistance of variable resistance R11 (namely, MTJ).
[0229] The sense current ISC which flows the memory cell of the MRAM cel MC 11 changes magnitude with the resistance (namely, value of variable resistance R11) of MTJ. Since it is RH>RL when the value of a sense current in case resistance of MTJ is RH and RL is set to IL and IH, IH>IL is realized.
[0230] Since a sense current flows in the MRAM cel MC 11, the electrical potential difference VS 1 of the source electrode (it connects with Multiplexer MUX) of the NMOS transistor MN13 falls rather than the drain electrical potential difference VDD.
[0231] This voltage drop detects data "1" as compared with reference voltage depending on magnetic tunnel resistance with the sense amplifier contained in Multiplexer MUX in this descent electrical potential difference.
[0232] When writing data "0" in the <B-2-4. write-in condition 0 (Wright 0)> MRAM cel MC 11 (the direction of spin is maintained), differing from the case of the write-in condition 1 is the point that the direction of the current which flows the subdevice-bit line BL1 becomes reverse. In order to realize this, make the NMOS transistors MN11 and MN14 into an OFF state, and let the NMOS transistors MN12 and MN13 be ON states.
[0233] Consequently, the current IBT which flows a bit line BL1 will flow toward a top from under drawing 27 .
[0234] When reading the data "0" written in the <B-2-5. read-out condition 0 (lead 0)> MRAM cel MC 11, actuation of the NMOS transistors MN11, MN12, MN13, and MN14 is the same as the read-out condition 1 (lead 1). However, electrical-potential-difference difference deltaV with the electrical potential difference VS 1 in case the electrical potential difference VS 1 of the source electrode of the NMOS transistor MN13 in case the data to read are "0", and the data to read are "1" becomes so large that the rate of change (RH-RL) of magnetic tunnel resistance / value of RL is large. Since the margin to reference voltage detectable [with a sense amplifier] becomes large so that electrical-potential-difference difference deltaV is large, detection becomes easy.
[0235] Here, the applied-voltage dependency of the rate of change of magnetic tunnel resistance is shown in drawing 29 . In drawing 29 , the rate of change {(RH-RL) /RL} of magnetic tunnel resistance is shown for the bias voltage impressed to an axis of abscissa at MTJ on an axis of ordinate. in addition, the property about the single MAG tunnel junction which has one layer of tunnel barrier layers which were explained to drawing 29 R> 9 until now, and which are MTJ -- a tunnel barrier layer -- two-layer -- ****** -- the property about a double MAG tunnel junction is shown collectively.
[0236] When the electrical potential difference impressed to a magnetic (single ****** duplex) tunnel junction is about 0.1V so that drawing 29 may show, the rate of change of magnetic tunnel resistance becomes max. Therefore, the electrical potential difference VW impressed to the subdevice-bit line BL1 at the time of read-out has a desirable electrical potential difference only with 0.1 V [higher than the electrical potential difference impressed to pn junction diode]. This electrical potential difference is realizable by adjusting the value of gate voltage VDD+delta VDD of the NMOS transistors MN11 and MN13.
[0237] Here, the configuration of a double MAG tunnel junction is explained using drawing 30 . As shown in drawing 30 , the double MAG tunnel junction has the configuration to which the laminating of the 1st antiferromagnetic substance layer AF 1, the ferromagnetic layer FM 1, the 1st tunnel barrier layer TB 1, the software ferromagnetic layer FMS, the 2nd tunnel barrier layer TB 2, and the 2nd antiferromagnetic substance layer AF 2 was carried out.
[0238] In such a configuration, when an electrical potential difference VX is impressed among the terminals TA and TB of the 1st and 2nd antiferromagnetic substance layers AF1 and AF2, VX / every

two electrical potential difference will be built over the 1st and 2nd tunnel barrier layers TB1 and TB2.
[0239] On the other hand, since an electrical potential difference VX will be built at a tunnel barrier thin film in the case of a single MAG tunnel junction, but the rate of change of magnetic tunnel resistance becomes so small that applied voltage is large, as the rate of change of magnetic tunnel resistance becomes large and the direction of a double MAG tunnel junction shows drawing 29 , a difference will arise in a property in a single MAG tunnel junction and a double MAG tunnel junction.
[0240] As explained beyond the <B-3. operation effectiveness>, according to MRAM of the gestalt 2 of operation concerning this invention Equip the both ends of the bit line of the MRAM cel array MCA, and a word line with the 1st control circuit CRW1 of train read-out / writing, and the 2nd control circuit CRW2 of train read-out / writing, and it sets to each. The 1st MOS transistor which connects a bit line and an electrical potential difference VDD (MN11, MN21, MN13, MN23), Since it has the 2nd MOS transistor (MN12, MN22, MN14, MN24) which connects a bit line and an electrical potential difference VSS The sense of the current which flows on a subdevice-bit line can be changed by changing an NMOS transistor, and the direction of the spin of the software ferromagnetic layer which constitutes MTJ can be changed into arbitration. In addition, since the NMOS transistor MN11, MN12 and MN21, MN22 and MN13, and MN14, MN23 and MN24 can change the connection place of the both ends of a bit line to an electrical potential difference VDD or an electrical potential difference VSS, they can call it a change means.
[0241] Moreover, since the 1st MOS transistor of the above of the 1st control circuit CRW1 of train read-out / writing is connected to the multiplexer MUX containing a sense amplifier, the electrical potential difference which originates in a sense current at the time of read-out of data can be outputted to Multiplexer MUX.
[0242] As a modification 1 of the gestalt 2 of operation concerning <B-4. modification 1> this invention, MRAM200 is shown in drawing 31 . In addition, MRAM200 has the almost same configuration as MRAM100 explained using drawing 27 . Differing instead of the NMOS transistors MN11, MN13, MN21, MN23, and QN11 in MRAM100, and QN21** The PMOS transistors MP11, MP13, MP21, MP23, QP11, and QP21 are formed. And the output of NAND gate ND11 is given to the gate electrode of the PMOS transistor MP 11 and the NMOS transistor MN12. The output of NAND gate ND12 is given to the gate electrode of the PMOS transistor MP 21 and the NMOS transistor MN22. The output of NAND gate ND13 is given to the gate electrode of an input, the PMOS transistor MP 13, and the NMOS transistor MN14. It is the point which gave the output of NAND gate ND14 to the gate electrode of the PMOS transistor MP 23 and the NMOS transistor MN24, and has communalized the gate input.
[0243] In MRAM100 shown in drawing 27 , since the electrical potential difference of VDD+delta VDD was impressed to the gate of MN21 and MN23 of the NMOS transistors MN11 and MN13 in the ON state, compared with the NMOS transistors MN12, MN14, MN22, and MN24 which only VDD requires for gate voltage, the burden placed on gate dielectric film may have become large.
[0244] However, in MRAM200 shown in drawing 31 , it is adopting the PMOS transistors MP11, MP13, MP21, and MP23, and since it is not necessary to impress the electrical potential difference more than VDD to the gate, the burden placed on gate dielectric film becomes small.
[0245] By moreover, the thing for which the PMOS transistors MP11, MP13, MP21, and MP23 are adopted Communalization of the NMOS transistors MN12, MN14, MN22, and MN24 and a gate input can be attained. The PMOS transistor MP 11 The NMOS transistor MN12, the PMOS transistor MP 21 and the NMOS transistor MN22, the PMOS transistor MP 13 and the NMOS transistor MN14, the PMOS transistor MP 23, and the NMOS transistor MN24 And an inverter (A driver and a buffer) are formed and power consumption can be reduced compared with MRAM100.
[0246] Drawing 32 is the timing chart of the various currents in MRAM200 at the time of read-out and writing, and an electrical potential difference.
[0247] In MRAM200, since each gate input of the PMOS transistors MP11 and MP13 and the NMOS transistors MN12 and MN14 is communalized, the timing chart of gate voltage V11 and V12 becomes the same, and the timing chart of gate voltage V13 and V14 becomes the same.

[0248] Moreover, although the timing chart of gate voltage VW1 and VW2 becomes the same since the gate input of the PMOS transistor QP 11 and the NMOS transistor QN12 is communalized (the same is said of the gate input of the PMOS transistor QP 21 and the NMOS transistor QN22), fundamental actuation is the same as MRAM100.
[0249] In addition, in this example, it is assumed as the electrical-potential-difference Vb= source electrical potential difference VSS and the electrical-potential-difference VW= drain electrical potential difference VDD. That is, when the property of MJT is the same as what was shown in drawing 29 , the drain electrical potential difference VDD is set as the value which added 0.1V to the electrical potential difference impressed to the pn junction diode of each MRAM cel almost equally.
[0250] Moreover, although not shown in drawing, read-out / write-in control circuit of MRAM 100 and 200 may be shared with an adjoining MRAM cel array. In this case, only a part to have shared does so the effectiveness of reducing equipment area.
[0251] As a modification 2 of the gestalt 2 of operation concerning <B-5. modification 2> this invention, MRAM300 is shown in drawing 33 . In addition, MRAM300 has the almost same configuration as MRAM200 explained using drawing 31 . Differing The PMOS transistor MP 11 And the NMOS transistor MN12, To each drain inter-electrode of the PMOS transistor MP 13 and the NMOS transistor MN14, the PMOS transistor MP 21 and the NMOS transistor MN22, the PMOS transistor MP 23, and the NMOS transistor MN24 The point which inserted the NMOS transistors MN15, MN16, MN25, and MN26, It is the point which inserted the NMOS transistors QN1 and QN2 in each drain inter-electrode of the PMOS transistor QP 11 and the NMOS transistor QN12, the PMOS transistor QP 21, and the NMOS transistor QN22.
[0252] In addition, the gate voltage of the NMOS transistors MN15, MN16, MN25, MN26, QN1, and QN2 is fixed to direct current voltage VGG.
[0253] The purpose of these NMOS transistors is reduction of leakage current. That is, BTBT(Band to band tunneling) TAT (Trap Assisted Tunneling), and the impact ionization (Impact Ionization) and SRH (Schockley-Read-hall process) to which the leakage current of MOSFET originates in the high electric field in a drain edge are the cause.
[0254] In order to reduce leakage current, the drain electrical potential difference given to the NMOS transistors MN12 and MN15 can be reduced by inserting the NMOS transistor MN15 in the drain inter-electrode of the PMOS transistor MP 11 and the NMOS transistor MN12, and setting the gate voltage of the NMOS transistor MN15 as predetermined direct current voltage (here electrical potential difference VGG) that what is necessary is just to reduce the electric field of a drain edge.
[0255] For example, an electrical potential difference VGG is set as VDD / 2+Vthn (threshold electrical potential difference of the NMOS transistor MN15), and it gives so that the NMOS transistor MN15 may always be made into an ON state. Then, when the NMOS transistor MN12 is turned on, it doubles with the NMOS transistor MN15. It will be in the condition that two resistance was connected to the serial. A resisted part Since the stress electrical potential difference (drain electrical potential difference VDD) which joins the NMOS transistors MN12 and MN15 comparatively more becomes equal, When not inserting the NMOS transistor MN15, compared with the leakage current only in the case of the NMOS transistor MN12, the total leakage current of MN12 and MN15 can be reduced sharply, and can reduce power consumption.
[0256] In addition, although having set the electrical potential difference VGG to VDD/2+Vthn is based on knowledge that the stress electrical potential difference which joins the NMOS transistors MN12 and MN15 by this setup becomes min equally, if power consumption is reduced in operation, it will not be limited to this electrical potential difference.
[0257] The above effectiveness is the same also in the NMOS transistors MN16, MN25, and MN26.
[0258] Moreover, also with the NMOS transistors QN1 and QN2 inserted in each drain inter-electrode of the PMOS transistor QP 11 and the NMOS transistor QN12, the PMOS transistor QP 21, and the NMOS transistor QN22, leakage current can be reduced sharply and power consumption can be reduced.

[0259] Moreover, although it assumed that a bidirectional current flowed to the bit line of a MRAM cel

array at the time of the writing of data, and the current of an one direction flowed to a word line, the current of an one direction flows to a bit line, and you may make it a bidirectional current flow to a word line in the above explanation.
[0260] Moreover, a component with ON / off properties, such as MOSFET, TFT (Thin Film Transistor), and a bipolar transistor, may be used instead of the pn junction diode of a MRAM cel.
[0261] MRAM concerning the gestalt 3 of operation of <gestalt 3 of C. operation> <description of gestalt of this operation> this invention is characterized by dividing the word line or bit line of a MRAM cel array into two or more sub word lines or sub bit lines.
[0262] That is, if the cross section of l and wiring is set [the resistivity of wiring] to S for the die length of rho and wiring, the wiring resistance R will be given by the formula (9) next.
[0263]
[Equation 9]

$$R=\rho\frac{l}{S} \quad \cdots(9)$$

[0264] Moreover, if the current which flows to wiring is set to I, power consumption P will be given by the degree type (10).
[0265]
[Equation 10]

$$P=RI^2=\rho\frac{lI^2}{S} \quad \cdots(10)$$

[0266] Therefore, if die-length l of wiring is shortened, it turns out that power consumption decreases. For example, if wiring is divided into two, power consumption will drop to 1/2, and if n division (however, n two or more integers) of is done, power consumption can drop to 1/n, can be written in in MRAM, and can reduce the power consumption at the time.
[0267] Moreover, an increment of the number of the memory cell linked to the same word line increases load-carrying capacity. Consequently, the time delay of the signal which transmits a word line increases, and the fault that rapid access is impossible arises.
[0268] However, in order that the number of the memory cell connected to the same wiring by dividing a word line into two or more sub word lines, and shortening the die length of wiring may decrease, load-carrying capacity is reduced. Consequently, a time delay can be shortened compared with the memory apparatus which does not divide a word line, and rapid access can be realized. This is the same also in a bit line. Hereafter, the concrete configuration of MRAM concerning the gestalt 3 of operation of this invention is explained.
[0269] A block diagram shows the configuration of MRAM400 which divided the word line into <division <C-1-1. equipment configuration> of C-1. word line> drawing 34 . As shown in drawing 34 , MRAM400 has two or more MRAM cel arrays 66.
[0270] The 2nd control circuit RRW2 of line read-out / writing connected to the 1st control circuit RRW1 of line read-out / writing and the 2nd edge at which each MRAM cel array 66 was connected to the 1st edge of two or more word lines 64, It has the 2nd control circuit CRW2 of train read-out / writing connected to the 1st control circuit CRW1 of train read-out / writing and the 2nd edge which were connected to the 1st edge of two or more bit lines 69.
[0271] In addition, although each above-mentioned control circuit presupposes that it is the same as that of MRAM 100-300 explained in the gestalt 2 of operation and the same sign is attached, it is not limited to these.
[0272] And corresponding to each MRAM cel array 66, two or more arrangement of the memory cell array selection line 70 connected to the train decoder which is not illustrated is carried out.
[0273] Moreover, the main word line 67 is connected to the output of two or more AND gates 62 which constitute a line decoder, respectively. In addition, the number of the main word line 67 is in agreement with the number of the word line of each MRAM cel array 66.

[0274] The AND gate 61 of 2 inputs which consider the memory cell array selection line 70 and the main word line 67 as an input is connected to the intersection of two or more memory cell array selection lines 70 and two or more main word lines 67, respectively, and the output is connected to the sub word line 64 through the 1st control circuit RRW1 of line read-out / writing. This sub word line 64 turns into a word line of each MRAM cel array 66.
[0275] Actuation of MRAM400 is explained below <C-1-2. equipment actuation>. For example, if one of the memory cell array selection lines 70 and one of the main word lines 67 are activated, the AND gate 61 connected to the activated memory cell array selection line 70 and the activated main word line 67 will activate the sub word line 64 connected to the output.
[0276] In this case, since the activated main word line 67 is not directly connected to a MRAM cel, the capacity of the MRAM cel which constitutes the MRAM cel array 66 is not contained in that capacity. Therefore, compared with the configuration which chooses a MRAM cel with one word line over two or more MRAM cel arrays, the capacity contained in a word line decreases sharply.
[0277] Furthermore, as for the sub word line 64 which crosses one MRAM cel array 66, with constituting so short that the delay (CR delay) resulting from capacity and resistance being disregarded, MRAM400 can essentially reduce the time amount which chooses a specific MRAM cel, and can raise the working speed of MRAM.
[0278] The capacity of a MRAM cel is explained here. As an example, the case where a MRAM cel consists of series connection of MTJ (magnetic tunnel junction) and pn junction diode is assumed.
[0279] In this case, the MRAM cel capacity CM turns into the capacity CTMR of MTJ, and capacity which connected the junction capacitance CD of pn junction diode to the serial, as shown in the following formulas (11).
[0280]
[Equation 11]

$$\frac{1}{C_M}=\frac{1}{C_{TMR}}+\frac{1}{C_D} \quad \cdots (11)$$

[0281] In MRAM400 shown in drawing 34 , since only the MRAM cel linked to the sub word line 64 in the selected MRAM cel array 66 is accessed, compared with the configuration which does not divide a word line, the current which flows between the sub word line 64 and bit lines 69 can decrease in proportion to the inverse number of the number of a MRAM cel array, and can reduce power consumption.
[0282] In addition, as a logic gate which controls the sub word line 64 in MRAM400, although the AND gate is used Even if it uses other logic gates, such as not the thing limited to the AND gate but a NAND gate, the NOR gate, and an XOR gate The same effectiveness as MRAM400 is done so in inputting into the above-mentioned logic gate combining the logic showing "High" of the memory cell array selection line 70 and the main word line 67, or "Low", and its reverse logic ("Low" or "High"). Here, it is equivalent to any [the high price of each signal level, or] of a low value they are with "High" of logic, and "Low."
[0283] A block diagram shows the configuration of MRAM500 which hierarchized the word line to <hierarchization <C-2-1. equipment configuration> of C-2. word line> drawing 35 . MRAM500 is equipped with n memory cell array groups 861-86n constituted by having m MRAM cel arrays 85 as shown in drawing 35 .
[0284] If the memory cell array group 861 is taken for an example, each MRAM cel array 85 The 2nd control circuit RRW2 of line read-out / writing connected to the 1st control circuit RRW1 of line read-out / writing and the 2nd edge which were connected to the 1st edge of two or more word lines 83, It has the 2nd control circuit CRW2 of train read-out / writing connected to the 1st control circuit CRW1 of train read-out / writing and the 2nd edge which were connected to the 1st edge of two or more bit lines 89.
[0285] And corresponding to each MRAM cel array 85, m memory cell array selection lines 911-91m connected to the train decoder which is not illustrated are arranged.

[0286] Moreover, the main word line 84 is connected to the output of two or more AND gates (subglobal decoder) 81, respectively. In addition, the number of the main word line 84 is in agreement with the number of the word line of each MRAM cel array 85.
[0287] The AND gate (local line decoder) 82 of 2 inputs which consider one of the main word lines 84 as an input with memory cell array selection lines [911-91m] any they are is connected to the intersection of the memory cell array selection lines 911-91m and two or more main word lines 84, respectively, and the output is connected to the sub word line 83 through the 1st control circuit RRW1 of line read-out / writing. This sub word line 83 turns into a word line of each MRAM cel array 85.
[0288] Moreover, it connects with the memory cell array group-selection line 901 of two or more subglobal decoders 81 in which all the 1st input was arranged corresponding to the memory cell array group 861 in common.
[0289] And each of the 2nd input is connected to the output of the Maine global decoder 80 through the global word line 87 of two or more subglobal decoders 81 connected to the output of two or more AND gates (Maine global decoder) 80.
[0290] The memory cell array group-selection lines 901-90n are wiring which is different in the global word line 87, and both are arranged so that it may cross.
[0291] In addition, other memory cell array groups have the same configuration as the memory cell array group 861, it connects with two or more subglobal decoders 81, respectively, and each subglobal decoders 81 of two or more are also connected to the memory cell array group-selection line.
[0292] That is, corresponding to memory cell array groups [861-86n] each, the memory cell array group-selection lines 901-90n are arranged, and the 2nd input of two or more subglobal decoders 81 connected to the memory cell array groups 861-86n, respectively is connected to the output of two or more Maine global decoders 80 through the global word line 87, respectively.
[0293] In addition, two or more Maine global decoders 80 are connected to the address signal track group 88.
[0294] Actuation of MRAM500 is explained below <C-2-2. equipment actuation>. It is chosen by the memory cell array group-selection lines 901-90n any they are, and two or more MRAM cel arrays 85 in 861-86n of memory cell array groups are chosen for the memory cell array groups 861-86n by the memory cell array selection lines 911-91m.
[0295] If actuation of the memory cell array groups 861-86n is the same as that of MRAM400 explained using drawing 34 , for example, one of the memory cell array selection line 911 and the main word lines 84 is activated, the AND gate 82 connected to the activated memory cell array selection line 911 and the main word line 84 will activate the sub word line 83 connected to the output.
[0296] In this case, since the capacity of the MRAM cel which constitutes the MRAM cel array 85 is not contained in the capacity of the activated main word line 84, compared with the conventional MRAM which had chosen the MRAM cel with one word line over two or more MRAM cel arrays, the capacity contained in a word line decreases sharply.
[0297] Moreover, for example, if one of the memory cell array group-selection line 901 and the global word lines 87 is activated, the AND gate 81 connected to the activated memory cell array group-selection line 901 and the global word line 87 will activate the main word line 84 connected to the output.
[0298] In this case, since the capacity of the MRAM cel array 85 which constitutes the memory cell array groups 861-86n is not contained in the capacity of the activated global word line 87, compared with the configuration which chooses a MRAM cel with one word line over two or more memory cell array groups, the capacity contained in a word line decreases sharply.
[0299] Therefore, compared with the conventional MRAM which does not hierarchize a word line, the current which flows between a word line 83 and bit lines 89 can decrease in proportion to the inverse number of the number of a memory cell array group, and it not only decreases in proportion to the inverse number of the number of a MRAM cel array, but it can reduce power consumption.
[0300] An example of the whole MRAM configuration with which the word line was hierarchized by <MRAM whole configuration by which C-2-3. word line was hierarchized> drawing 36 is shown. In

drawing 36 , MRAM equipped with four memory cell array groups 861-864 constituted by having four MRAM cel arrays 851-854 is shown, and four memory cell array group-selection lines 901-904 are arranged corresponding to each of four memory cell array groups 861-864. Moreover, in each memory cell array group, four memory cell array selection lines 911-914 are arranged corresponding to four MRAM cel arrays 851-854.

[0301] In addition, in drawing 36 , each configuration of MRAM cel array 85 grade is expressed with a simple block, and shows typically each wiring path of global word line 87 grade by the arrow head. Drawing 36 shows that the so-called word line is hierarchized.

[0302] A block diagram shows the configuration of MRAM600 which divided the bit line into <division <C-3-1. equipment configuration> of C-3. bit line> drawing 37 . As shown in drawing 37 , MRAM600 has two or more MRAM cel arrays 166.

[0303] The 2nd control circuit RRW2 of line read-out / writing connected to the 1st control circuit RRW1 of line read-out / writing and the 2nd edge at which each MRAM cel array 166 was connected to the 1st edge of two or more word lines 160, It has the 2nd control circuit CRW2 of train read-out / writing connected to the 1st control circuit CRW1 of train read-out / writing and the 2nd edge which were connected to the 1st edge of two or more bit lines 164.

[0304] In addition, although the above-mentioned control circuit presupposes that it is the same as that of MRAM 100-300 explained in the gestalt 2 of operation and the same sign is attached, it is not limited to these.

[0305] And corresponding to each MRAM cel array 166, two or more arrangement of the memory cell array selection line 170 connected to the line decoder which is not illustrated is carried out.

[0306] Moreover, the Maine bit line 167 is connected to the output of two or more AND gates 162 which constitute a train decoder, respectively. In addition, the number of the Maine bit line 167 is in agreement with the number of the bit line of each MRAM cel array 166.

[0307] NAND gate 161 of 2 inputs which consider the memory cell array selection line 170 and the Maine bit line 167 as an input is connected to the intersection of two or more memory cell array selection lines 170 and two or more Maine bit lines 167, respectively, and the output is connected to the sub bit line 164 through the 1st control circuit CRW1 of train read-out / writing. The ** sub bit line 164 turns into a bit line of each MRAM cel array 166.

[0308] Actuation of MRAM600 is explained below <C-3-2. equipment actuation>. For example, if one of the memory cell array selection lines 170 and one of the Maine bit lines 167 are activated, NAND gate 161 connected to the activated memory cell array selection line 170 and the activated Maine bit line 167 will activate the sub bit line 164 connected to the output.

[0309] In this case, since the activated Maine bit line 167 is not directly connected to a MRAM cel, the capacity of the MRAM cel which constitutes the MRAM cel array 166 is not contained in that capacity. Therefore, compared with the configuration which chooses a MRAM cel with one bit line over two or more MRAM cel arrays, the capacity contained in a bit line decreases sharply.

[0310] Furthermore, since the sub bit line 164 which crosses one MRAM cel array 166 can be done so short that the delay (CR delay) resulting from capacity and resistance can be disregarded, MRAM600 can essentially reduce the time amount which chooses a specific MRAM cel, and can raise the working speed of MRAM.

[0311] Although the overlapping explanation is omitted since the capacity of a MRAM cel is explained using a formula (11) Since only the MRAM cel which has connected with the sub bit line 164 in the selected MRAM cel array 166 in MRAM600 shown in drawing 37 is accessed Compared with the configuration which does not divide a bit line, the current which flows between the sub bit line 164 and word lines 169 can decrease in proportion to the inverse number of the number of a MRAM cel array, and can reduce power consumption.

[0312] In addition, as a logic gate which controls the sub bit line 164 in MRAM600, although the NAND gate is used Even if it uses other logic gates, such as not the thing limited to a NAND gate but the AND gate, the NOR gate, and an XOR gate The same effectiveness as MRAM600 is done so in inputting into the above-mentioned logic gate combining the logic showing "High" of the memory cell

array selection line 170 and the Maine bit line 167, or "Low", and its reverse logic ("Low" or "High"). Here, it is equivalent to any [the high price of each signal level, or] of a low value they are with "High" of logic, and "Low."
[0313] A block diagram shows the configuration of MRAM700 which hierarchized the bit line to <hierarchization <C-4-1. equipment configuration> of C-4. bit line> drawing 38 . MRAM700 is equipped with n memory cell array groups 1861-186n constituted by having m MRAM cel arrays 185 as shown in drawing 38 .
[0314] If the memory cell array group 1861 is taken for an example, each MRAM cel array 185 The 2nd control circuit RRW2 of line read-out / writing connected to the 1st control circuit RRW1 of line read-out / writing and the 2nd edge which were connected to the 1st edge of two or more word lines 189, It has the 2nd control circuit CRW2 of train read-out / writing connected to the 1st control circuit CRW1 of train read-out / writing and the 2nd edge which were connected to the 1st edge of two or more bit lines 183.
[0315] And corresponding to each MRAM cel array 185, m memory cell array selection lines 1911-191m connected to the line decoder which is not illustrated are arranged.
[0316] Moreover, the Maine bit line 184 is connected to the output of two or more AND gates (subglobal decoder) 181, respectively. In addition, the number of the Maine bit line 184 is in agreement with the number of the bit line of each MRAM cel array 185.
[0317] The AND gate (local train decoder) 182 of 2 inputs which consider one of the Maine bit lines 184 as an input with memory cell array selection lines [1911-191m] any they are is connected to the intersection of the memory cell array selection lines 1911-191m and two or more Maine bit lines 184, respectively, and the output is connected to the sub bit line 183 through the 1st control circuit CRW1 of train read-out / writing. This sub bit line 183 turns into a word line of each MRAM cel array 185.
[0318] Moreover, it connects with the memory cell array group-selection line 1901 of two or more subglobal decoders 181 in which all the 1st input was arranged corresponding to the memory cell array group 1861 in common.
[0319] And each of the 2nd input is connected to the output of the Maine global decoder 180 through the global bit line 187 of two or more subglobal decoders 181 connected to the output of two or more AND gates (Maine global decoder) 180.
[0320] The memory cell array group-selection lines 1901-190n are wiring which is different in the global bit line 187, and both are arranged so that it may cross.
[0321] In addition, other memory cell array groups have the same configuration as the memory cell array group 1861, it connects with two or more subglobal decoders 181, respectively, and each subglobal decoders 181 of two or more are also connected to the memory cell array group-selection line.

[0322] That is, corresponding to memory cell array groups [1861-186n] each, the memory cell array group-selection lines 1901-190n are arranged, and the 2nd input of two or more subglobal decoders 181 connected to the memory cell array groups 1861-186n, respectively is connected to the output of two or more Maine global decoders 180 through the global bit line 187, respectively.
[0323] In addition, two or more Maine global decoders 180 are connected to the address signal track group 188.
[0324] Actuation of MRAM700 is explained below <C-4-2. equipment actuation>. It is chosen by the memory cell array group-selection lines 1901-190n any they are, and two or more MRAM cel arrays 185 in 1861-186n of memory cell array groups are chosen for the memory cell array groups 1861-186n by the memory cell array selection lines 1911-191m.
[0325] If actuation of the memory cell array groups 1861-186n is the same as that of MRAM600 explained using drawing 37 , for example, one of the memory cell array selection line 1911 and the Maine bit lines 184 is activated, the AND gate 182 connected to the activated memory cell array selection line 1911 and the Maine bit line 184 will activate the sub bit line 183 connected to the output.
[0326] In this case, since the capacity of the MRAM cel which constitutes the MRAM cel array 185 is not contained in the capacity of the activated Maine bit line 184, compared with the conventional

MRAM which had chosen the MRAM cel with one bit line over two or more MRAM cel arrays, the capacity contained in a bit line decreases sharply.
[0327] Moreover, for example, if one of the memory cell array group-selection line 1901 and the global bit lines 187 is activated, the AND gate 181 connected to the activated memory cell array group-selection line 1901 and the global bit line 187 will activate the Maine bit line 184 connected to the output.
[0328] In this case, since the capacity of the MRAM cel array 185 which constitutes the memory cell array groups 1861-186n is not contained in the capacity of the activated global bit line 187, compared with the configuration which chooses a MRAM cel with one bit line over two or more memory cell array groups, the capacity contained in a bit line decreases sharply.
[0329] Therefore, compared with the conventional MRAM which does not hierarchize a bit line, the current which flows between a bit line 183 and word lines 189 can decrease in proportion to the inverse number of the number of a memory cell array group, and it not only decreases in proportion to the inverse number of the number of a MRAM cel array, but it can reduce power consumption.
[0330] In addition, although the example which set in the gestalt 3 of the operation explained above, and was divided and hierarchized about each of a word line and a bit line was explained, it is good also as a configuration which hierarchized both the configuration which combined these and divided both the word line and the bit line or the word line, and the bit line. By taking such a configuration, reduction of the further power consumption and the working speed of MRAM can be raised further.
[0331] MRAM concerning the gestalt 4 of operation of <gestalt 4 of D. operation> <description of gestalt of this operation> this invention is characterized by package-eliminating or package writing in the stored data of two or more MRAM cels using the field generated in the inductor.
[0332] <D-1. equipment configuration> drawing 39 is the perspective view showing the configuration of MRAM800 concerning the gestalt 4 of operation of this invention. In drawing 39 , bit lines 4, 5, and 6 are arranged in parallel mutually, the MRAM cel MC is formed in each intersection across which it faces with a word line and a bit line, and the MRAM cel array MCA 1 is constituted so that it may cross in the upper part of the word lines 1, 2, and 3 arranged in parallel mutually.
[0333] Although the explanation which explains the configuration of the MRAM cel MC using drawing 1 , and overlaps is omitted, the direction of the easy axis of the software ferromagnetic layer which constitutes the MRAM cel MC is the extension direction of each word line so that it may ****.
[0334] And the coiled form inductor ID is arranged so that the MRAM cel array MCA 1 may be surrounded.
[0335] Inductor ID connects metal wiring to a coiled form, is constituted, and is rolled about along the direction where word lines 1-3 extend.
[0336] And it connects with the inductor drive circuit (not shown) which can pass a current bidirectionally, and the both ends of Inductor ID have the composition that the direction of the field generated to the field surrounded by Inductor ID can be changed by changing the sense of the current passed to Inductor ID. In addition, the field generated by Inductor ID is mostly in agreement in the direction of the easy axis of the software ferromagnetic layer which constitutes the MRAM cel MC where word lines 1-3 extend, i.e., the direction.
[0337] Therefore, when performing package elimination or the package writing of data to two or more MRAM cels MC of the MRAM cel array MCA 1, the directions of the spin of a software ferromagnetic layer can be changed in the predetermined direction for a current all at once from an inductor drive circuit at Inductor ID by the sink and the field to generate.
[0338] in addition, in drawing 39 , for convenience, although the memory cell array of three-line three trains is shown, the size of a row and column is not the thing of explanation limited to this -- there is nothing.
[0339] moreover, Inductor ID, word lines 1-3, a bit line 4 - 6 grades -- each -- a conductor -- between lines, although the gas or the solid insulator is arranged, by drawing 39 , the display is omitted for convenience.
[0340] Moreover, in drawing 39 , for convenience, although the pitch of the winding of Inductor ID is

shown more greatly than the pitch of the MRAM cel array MCA 1, it is not the thing of explanation limited to this.
[0341] Moreover, what is necessary is to be the configuration of having the double MAG tunnel junction which especially limitation does not have in the configuration of the MRAM cel MC, for example, was explained using drawing 30 , and just to have at least one magnetic tunnel junction. For example, the memory cell which carried out the loop formation of the magnetic flux to at least one magnetic tunnel junction by static magnetism association, and was equipped with the magnetic substance / non-magnetic material / magnetic-substance structure is sufficient.
[0342] Moreover, an inductor does not need to be a coiled form if the field which is in agreement in the direction of the easy axis of a software ferromagnetic layer can be generated.
[0343] drawing 40 which is a sectional view in the A-A line in drawing 39 here - drawing 42 -- using -- ****** explanation of MRAM800 of operation -- it carries out. In addition, a different pitch from drawing 39 of explanation shows the winding pitch of Inductor ID for convenience.
[0344] Drawing 40 shows an example of the condition before package elimination. As shown in drawing 40 , the MRAM cel MC has the configuration by which the magnetic tunnel junction (MTJ) was arranged in the upper part of the pn junction diode PN. And the direction of the spin of the software ferromagnetic layer 22 which constitutes the MRAM cel MC of the lower part of a bit line 5 has turned to the left toward drawing, and the direction of the spin of other MRAM cels MC has turned to the right. And Inductor ID is grounded in the state of standby of the condition ID which does not carry out package elimination actuation and package write-in actuation, i.e., an inductor. The effectiveness of intercepting an external noise and protecting the MRAM cel array MCA 1 by this is done so.
[0345] Drawing 41 shows an example of the condition of package elimination. If the signal of package elimination is inputted into an inductor drive circuit, a rightward field will occur so that the current of the 1st direction may flow and **** to Inductor ID. That the field inside an inductor leaks to the exterior decreases, and a field can be efficiently generated, so that the pitch of Inductor ID is narrow at this time.
[0346] Here, if the direction of the spin showing elimination is made into facing the right in drawing, the spin of the software ferromagnetic layer 22 of all the MRAM cels MC will turn [coincidence] to right-hand side, and package elimination of the data will be carried out by the field of the right generated inside the inductor.
[0347] Drawing 42 shows an example of the condition of package writing. If the signal of package writing is inputted into an inductor drive circuit, a leftward field will occur so that a current may flow and **** in the 2nd direction opposite to the 1st direction to Inductor ID.
[0348] Here, if the direction of the spin showing writing is made into the facing the left in drawing, by the field of the left generated inside the inductor, the spin of the software ferromagnetic layer 22 of all the MRAM cels MC will turn [coincidence] to the left, data will bundle up, and it will be written in.
[0349] The <D-2. operation effectiveness> When package elimination or the same data is put in block and it writes in the stored data of two or more MRAM cels, time amount is taken by the approach of choosing the address in detail, and eliminating or writing in stored data with a word line and a bit line, and power consumption is also large.
[0350] On the other hand, since package elimination or the package writing of the data of two or more MRAM cels can be carried out, it can process in a short time and a field is efficiently generated by Inductor ID, there is also little power consumption and it can be managed with MRAM by the gestalt of this operation.
[0351] <D-3. modification> In order to package-eliminate or package write in the stored data of two or more MRAM cels, the configuration of those other than an inductor can also be taken.
[0352] The flat-surface configuration of MRAM900 is shown in drawing 43 as a modification of the gestalt 4 of this operation. In addition, in drawing 43 , for convenience, although the MRAM cel array MCA 2 of four-line four trains is shown, the size of a row and column is not the thing of explanation limited to this.
[0353] As shown in drawing 43 , the flash plate bit line FBL and the flash plate word line FWL for batch processing of data are arranged in the upper and lower sides of the MRAM cel array MCA 2.

[0354] The flash plate bit line FBL and the flash plate word line FWL are formed corresponding to the field whole region where two or more bit lines BL1 and word lines WL1 were arranged, respectively, and the plane view configuration has all become rectangle-like in drawing 43 .
[0355] It has the composition that a bit line BL1 crosses in the upper part of a word line WL1 in drawing 43 , and the MRAM cel MC is arranged between the both lines of the intersection of a word line WL1 and a bit line BL1.
[0356] And the flash plate word line FWL is arranged by the lower part of a word line WL1, and the flash plate bit line FBL is arranged in the upper part of a bit line BL1. In addition, in drawing 43 , the topmost flash plate bit line FBL is deleted partially for convenience, and is shown.
[0357] It can set to drawing 43 and the cross-section configuration in an A-A line and a B-B line is shown in drawing 44 and drawing 45 , respectively.
[0358] As shown in drawing 45 , the MRAM cel MC has the configuration by which the magnetic tunnel junction (MTJ) was arranged in the upper part of the pn junction diode PN.
[0359] Thus, up and down, the flash plate bit line FBL and the flash plate word line FWL are arranged, on the occasion of package elimination or package writing, it is the thing of the MRAM cel array MCA 2 for which the current of the predetermined direction is passed to the flash plate bit line FBL and the flash plate word line FWL, and package elimination or package writing can be realized by turning the spin of the software ferromagnetic layer of all the MRAM cels MC in the same direction as coincidence.

[0360] In addition, what is necessary is just to make the direction of the current passed for package elimination or package writing the same as a bit line BL and the direction of a current passed word line WL in the flash plate bit line FBL and the flash plate word line FWL, in case elimination or the writing of data is separately performed in the MRAM cel MC.
[0361] In addition, for the flash plate bit line FBL and the flash plate word line FWL, you may have both and only one of the two is. Namely, since the field to generate is proportional to the magnitude of a current, if many currents are passed, at least one side is possible for reversal of spin.
[0362] In addition, total of the current which needs the direction which generates the field of the same magnitude by the both line to reverse spin can be small performed using both the flash plate bit line FBL and the flash plate word line FWL.
[0363] Moreover, at the time of standby of the condition FBL which does not carry out package elimination actuation and package write-in actuation, i.e., a flash plate bit line, and the flash plate word line FWL, the noise resulting from an external field and electric field is covered by grounding the flash plate bit line FBL and the flash plate word line FWL, and the effectiveness of protecting the MRAM cel array MCA 2 is done so.
[0364] In addition, in MRAM900 explained above, although the configuration which has one MRAM cel array MCA 2 was shown, a MRAM cel array is applicable also in the configuration which it has. It is shown in drawing 46 , using the configuration concerned as MRAM900A.
[0365] As shown in drawing 46 , in MRAM900A, two or more MRAM cel arrays MCA 2 are arranged in the shape of a matrix, and the global flash plate bit line GBL and the global flash plate word line GWL for batch processing of data are arranged in the upper and lower sides of the array of the MRAM cel array MCA 2 in the shape of a matrix so that it may correspond to the array of the MRAM cel array MCA 2.
[0366] Although the global flash plate bit line GBL and the global flash plate word line GWL have the same function as the flash plate bit line FBL and the flash plate word line FWL which are shown in drawing 43 and omit explanation, since it is used common to two or more MRAM cel arrays MCA 2, they have changed the name.
[0367] In addition, the 1st control circuit RRW1 of line read-out / writing explained in drawing 27 , drawing 31 , and drawing 33 , the 2nd control circuit RRW2 of line read-out / writing and the 1st control circuit CRW1 of train read-out / writing, and the 2nd control circuit CRW2 of train read-out / writing may be used for the control circuit of the flash plate bit line FBL explained above and the flash plate word line FWL, the global flash plate bit line GBL, and the global flash plate word line GWL.

[0368] Moreover, it sets like MRAM900A shown in drawing 46 in the configuration which has two or more MRAM cel arrays MCA 2. Since a current may flow also in the MRAM cel array MCA 2 of not choosing in the same train as the MRAM cel array MCA 2 set as the object of package elimination or package writing, and the same line The divided word line which was explained using drawing 34 - drawing 38 in order to reduce the consumed electric current, The technical thought of the divided bit line, the hierarchized word line, and the hierarchized bit line may be applied to the global flash plate bit line GBL and the global flash plate word line GWL.
[0369] Using LC resonance of an inductor and a capacitor, MRAM concerning the gestalt 5 of operation of <gestalt 5 of E. operation> <description of gestalt of this operation> this invention recycles a current, and is characterized by using for rewriting of at least 1 times or more of stored data.
[0370] <E-1. equipment configuration> drawing 47 is drawing showing the flat-surface configuration of MRAM1000 concerning the gestalt 5 of operation of this invention. A multiplexer MUX1 is connected to the 1st edge of two or more bit lines BL1 of the MRAM cel array MCA 3 in drawing 47 , and the multiplexer MUX2 is connected to the 2nd edge. Moreover, the drain electrical potential difference VDD is given to the 1st edge of two or more word lines WL1, and the NMOS transistor QN1 is connected to each 2nd edge of two or more word lines WL1.
[0371] Moreover, two or more NMOS transistors QM1 prepared corresponding to the number of two or more bit lines BL1 are connected to a multiplexer MUX1, and the capacitor CP 1 is connected to the source electrode of each NMOS transistor QM1.
[0372] Moreover, the multiplexer MUX2 is constituted so that one inductor ID 1 may be connected to two bit lines BL1, and the inductor ID 1 of the number equivalent to the one half of the total of two or more bit lines BL1 is connected to the multiplexer MUX2 as a result.
[0373] In addition, although the train decoder explained using drawing 26 , the line decoder, and the control circuit are connected to the bit line BL1 and the word line WL1, since they have thin relation with the gestalt of this operation and are simplification of explanation, illustration and explanation are omitted.
[0374] <E-2. equipment actuation>, next actuation of MRAM1000 are explained. In addition, the sign of BL1a and BL1b may be attached and distinguished to a bit line BL1 for convenience below.
[0375] First, the word line WL1 including the selection address is chosen, and a direct current IDC flows to the selection word line WL1 concerned.
[0376] Next, the bit line BL1 including the selection address is chosen by the multiplexer MUX1, and writes in via the subdevice-bit line BL1a concerned, and a current I1 flows into a multiplexer MUX2. In this case, the inductor ID 1 connected to subdevice-bit line BL1a is chosen by the multiplexer MUX2, and the energy of the write-in current I1 is saved as a magnetic field in an inductor ID 1.
[0377] If another bit line BL1 connected to the above-mentioned inductor ID 1 is chosen by the multiplexer MUX2, the write-in current I1 which flowed can flow to the subdevice-bit line BL1b concerned, and can reuse an inductor ID 1 as a current I2.
[0378] This current I2 is stored in the vacant capacitor CP 1 as a charge via a multiplexer MUX1, and can be theoretically written in any number of times by connecting multiplexers MUX1 and MUX2 suitably again.
[0379] In addition, according to are recording of the charge to a capacitor CP 1, and the timing of emission of the charge from a capacitor CP 1, on-off control of two or more NMOS transistors QM1 is carried out, and on-off control of two or more NMOS transistors QN1 is carried out to a word line WL1 according to the timing which passes a direct current IDC.
[0380] As explained beyond the <E-3. operation effectiveness>, the power consumption at the time of writing can be reduced by recycling the write-in current in a bit line BL1 using LC resonance of an inductor ID 1 and a capacitor CP 1.
[0381] As a modification of the gestalt of <E-4. modification> book operation, the flat-surface configuration of MRAM1100 is shown in drawing 48 . In MRAM1100, in addition to the configuration of MRAM1000 shown in drawing 47 , a multiplexer MUX3 is connected to the 1st edge of two or more word lines WL1 of the MRAM cel array MCA 3, and the multiplexer MUX4 is connected to the 2nd

edge.

[0382] Moreover, two or more NMOS transistors QN1 prepared corresponding to the number of two or more word lines WL1 are connected to a multiplexer MUX3, and the capacitor CP 2 is connected to the source electrode of each NMOS transistor QN1.

[0383] Moreover, the multiplexer MUX4 is constituted so that one inductor ID 2 may be connected to two word lines WL1, and the inductor ID 2 of the number equivalent to the one half of the total of two or more bit lines WL1 is connected to the multiplexer MUX4 as a result.

[0384] In MRAM1100 of such a configuration, the write-in current not only in the write-in current in a bit line BL1 but the word line WL1 can be recycled using LC resonance of an inductor ID 2 and a capacitor CP 2, and the power consumption resulting from consumption of a write-in current can be reduced further.

[0385] In addition, since recycle actuation of an inductor ID 2 and the write-in current by LC resonance of a capacitor CP 2 is the same as that of it by LC resonance of an inductor ID 1 and a capacitor CP 1, explanation is omitted.

[0386] Moreover, it is compensated by the general current detection mold compensating network established in multiplexers MUX1-MUX4 about the current consumed in an inductor ID 1 and a capacitor CP 1, an inductor ID 2, and a capacitor CP 2.

[0387] In addition, what is necessary is just to use the spiral inductor formed by coiling wiring around a curled form and carrying out a time as inductors ID1 and ID2, for example.

[0388] The configuration shown in drawing 47 and drawing 48 is an example, and if it can be written in using LC resonance and recycle of a current can be aimed at, it will not be limited to the above-mentioned configuration.

[0389] The magnetic-substance substrate concerning the gestalt 5 of operation of <gestalt 6 of F. operation> <description of gestalt of this operation> this invention is characterized by forming the multilayers used as a magnetic tunnel junction (MTJ) on a principal plane beforehand.

[0390] The cross-section configuration of the magnetic-substance substrate concerning the gestalt 5 of the operation of this invention to <F-1. substrate configuration> drawing 49 is shown. In drawing 49 , all over the principal plane of silicon substrate SB, the insulator layers IL 1, such as silicon oxide or a silicon nitride, are arranged, and the conductor layer ML1 which serves as a word line or a bit line behind is arranged on it.

[0391] The laminating of the p-type silicon layer SF 2 which has n mold silicon layer SF 1 which has comparatively high-concentration n mold impurity, and comparatively high-concentration p mold impurity is carried out to the upper part of a conductor layer ML1. Two-layer [this] serves as pn junction diode behind.

[0392] And the tungsten layer STD which serves as a tungsten stud behind is formed in the upper part of the p-type silicon layer SF 2, and the multilayers which serve as MTJ behind are arranged on the tungsten layer STD.

[0393] Namely, the template layer TPL which consists of platinum (Pt) sequentially from the bottom, The initial ferromagnetic layer IFL (4nm of thickness) which consists of permalloys of nickel81Fe19, The diamagnetic-material layer AFL (10nm of thickness) which consists of Mn54Fe(s)46, The ferromagnetic layer FFL (8nm of thickness) which consists of permalloys of CoFe or nickel81Fe19, It has the contact layer CL which consists of software ferromagnetic layers FML and Pt which consist of multilayers of CoFe of the tunnel barrier layer TBL which consists of aluminum 2O3, and 2nm of thickness, and nickel81Fe19 of 20nm of thickness.

[0394] Moreover, the conductor layer ML2 used as a word line or a bit line is arranged in the upper part of the contact layer CL, and the insulator layer IL 2 is arranged in behind as antioxidizing film of a metal layer at the topmost part.

[0395] If such a magnetic-substance substrate is sold, a user can form the MRAM cel array MCA 1 as shown in drawing 39 R> 9 by carrying out patterning by argon ion milling, using a photoresist mask.

[0396] The <F-2. operation effectiveness> A board maker sells the magnetic-substance substrate with which the multilayers which serve as pn junction diode and MTJ beforehand were formed on the

principal plane in this way, and it is using the magnetic-substance substrate concerned, and a user can prepare a mere silicon substrate, can skip a production process compared with the case where multilayers are formed on the principal plane, and can reduce a manufacturing cost.
[0397] The magnetic-substance substrate with which the multilayers used as pn junction diode and MTJ were beforehand formed on the principal plane of a SOI (Silicon On Insulator) substrate at <F-3. modification> drawing 50 is shown.
[0398] In drawing 50 , it embeds on silicon substrate SB, an oxide film BX is arranged, and the SOI layer SI is arranged on the embedding oxide film BX. And on the SOI layer SI, the same multilayers as being shown drawing 49 are arranged.
[0399] As explained using drawing 31 and drawing 33 , MOSFET is required for MRAM. And since parasitic capacitance can be reduced if MOSFET is formed on a SOI layer, the working speed of MOSFET can be made quick and the working speed of MRAM can also be made quick as a result.
[0400] In addition, in the gestalt 6 of the operation explained above, although the multilayers used as a magnetic tunnel junction showed the configuration deposited on the bulk silicon substrate or the SOI substrate and called it the magnetic-substance substrate, the multilayers (multilayers of the thin film magnetic substance) used as a magnetic tunnel junction may be deposited on a glass substrate or a resin substrate, and the class of substrate used as a foundation is not limited to a semi-conductor substrate.
[0401] Therefore, in this invention, the configuration which deposited the multilayers of the thin film magnetic substance by using a certain substrate as a foundation is called the thin film magnetic-substance substrate.
[0402] MRAM concerning the gestalt 7 of operation of <gestalt 7 of G. operation> <description of gestalt of this operation> this invention is characterized by being formed on various functional block formed on the principal plane of a substrate.
[0403] <G-1. equipment configuration> First, in order to explain a difference with the gestalt of this operation, a block diagram shows the configuration of the conventional common semiconductor memory to drawing 51 .
[0404] In drawing 51 , the train address buffer 31, the train decoder 32, train read-out / write-in control circuit 33, the line address buffer 34, the line decoder 35, and line read-out / write-in control circuit 36 are arranged in the perimeter of the memory cell array 31 as a circumference circuit of the memory cell array 31.
[0405] Moreover, the input output buffer which transmits and receives a signal with the equipment exterior as other functional block (I/O buffer), The above-mentioned signal is larger than a value of standard, or And (overshoot), When small (undershoot), restore to the ESD (Electric Static Discharge) circuit 44 returned to a value of standard, and the signal modulated, or A signal The function to modulate The modulation/demodulator circuit which it has (Modulator/Demodulator) Agency of transfer of the data between DSP (Digital Signal Processing)42 and the memory cell array 31 which have the function to process 43 and a digital signal, and a circumference circuit (data are held temporarily or) Perform taking the synchronization of transmission and reception of the data between a circumference circuit and the memory cell array 31 etc. It has the input/output controller (I/O controller 53) which controls I/O of the data of the first cache 51 and the second cache 52, and the memory cell array 31, and CPU (Micro processor)41 which performs data processing of data.
[0406] With the conventional semiconductor memory, for example, DRAM, SRAM, and EEPROM, since MOSFET was included in a memory cell array, it needed to form on the principal plane of a semi-conductor substrate, and the memory cell array was formed as a result on the principal plane front face of the same semi-conductor substrate as each functional block.
[0407] A block diagram shows the configuration of MRAM1200 which starts the gestalt 7 of the operation of this invention to drawing 52 here.
[0408] The MRAM cel array MCA is overlapped and arranged in the upper part of the arrangement field of the circumference circuit CAB of the MRAM cel array MCA, i.e., a train address buffer, the train decoder CD, train read-out / write-in control circuit CRW, the line address buffer RAB, the line decoder RD, and the line read-out / write-in control circuit RRW in drawing 52 .

[0409] In addition, since the configuration of a circumference circuit is the same as the configuration explained using drawing 26 and it is the same as that of the semiconductor memory from the former about other functional block, explanation is omitted.
[0410] Since the <G-2. operation effectiveness> MRAM cel array MCA contains only pn junction diode as a semiconductor device excluding MOSFET in the interior as explained using drawing 28 , drawing 31 , and drawing 33 , a formation field is not limited to the principal plane front face of a substrate.
[0411] Therefore, equipment area is reducible by forming various functional block on the principal plane front face of a substrate, and forming the MRAM cel array MCA in the upper layer including the configuration of those other than the MRAM cel array MCA, i.e., the circumference circuit of the MRAM cel array MCA.
[0412] A block diagram shows the configuration of MRAM1300 to <G-3. modification> drawing 53 as a modification of the gestalt of this operation.
[0413] As shown in drawing 53 , the MRAM cel array MCA is overlapped and arranged in the whole upper part of the field in which a circumference circuit and various functional block were formed in MRAM1300.
[0414] Thus, while the degree of freedom of selection of the arrangement location of the MRAM cel array MCA or magnitude will increase and being able to reduce equipment area by forming the MRAM cel array MCA, a circumference circuit, and various functional block in a separate layer, the selectivity of an equipment layout can also be raised.
[0415] MRAM concerning the gestalt 8 of operation of <gestalt 8 of H. operation> <description of gestalt of this operation> this invention is characterized by taking the gestalt of MCP (Multi Chip Package) which used a MRAM cel array, and the circumference circuit and various functional block of a MRAM cel array as the separate semiconductor chip, and was contained in one package by using both chips as a module.
[0416] The maximum formation temperature at the time of manufacture of the circumference circuit of a <introduction> MRAM cel array and various functional block is about 1000-1200 degrees C, and on the other hand, the maximum formation temperature at the time of manufacture of a MRAM cel array is decided by Curie temperature, and is about 400-700 degrees C.
[0417] When forming both on the same semi-conductor substrate, in order to prevent the fault by the difference in formation temperature, the maximum formation temperature forms the MRAM cel array in the wiring process which is about 400-700 degrees C.
[0418] Therefore, in the production process of MRAM, the process became sequential, and there was a problem which requires a manufacturing cost.
[0419] On the other hand, in these days, the MCP structure which contained two or more semiconductor chips is being used for one package. When it was MRAM of a configuration of the artificer etc. having used a MRAM cel array, and the circumference circuit and various functional block of a MRAM cel array as the separate semiconductor chip, and having contained in one package by using both chips as a module in view of such the present condition, the above-mentioned problem reached the conclusion with solution, but in order to have obtained MRAM of MCP structure actually, it resulted in recognition that it cannot respond to MRAM, with the conventional package structure.
[0420] After explaining the technical problem for realizing MRAM of MCP structure hereafter, the configuration of MRAM2000 concerning the gestalt 8 of operation is explained.
[0421] As the mounting approach of the semiconductor chip which contains > semiconductor device about the MCP structure of the <H-1. former, although QFP (Quad FlatPackage) was used conventionally, there was a trouble that a component-side product was large. Then, CSP (Chip Size Package) which can be managed with the component-side product of the almost same magnitude as a chip area is beginning to be used in recent years. Since this mounting approach can be managed with a far small component-side product compared with QFP, it is used for LSI for cellular phones, DRAM for PC (Personal Computer), etc.
[0422] A sectional view shows an example of the configuration of conventional CSP to drawing 54 . In drawing 54 , a semiconductor chip 122 is contained inside the package 129 of a cube type, and the

bottom principal plane of a semiconductor chip 122 is covered with the passivation film 123, and is protected from the external environment.
[0423] The passivation film 123 consists of insulator layers, such as a silicon nitride film and an acid silicon nitride film, two or more openings are prepared in the passivation film 123, and the chip electrode 132 used as the input/output terminal of a semiconductor chip 122 has composition which penetrates the passivation film 123.
[0424] As for a package 129, box-like [of closed-end ****] is inserted in a semiconductor chip 122 from nothing and its opening. Here, finally opening of a package 129 is covered by the base substrate 134. The body of the base substrate 134 concerned consists of insulating materials, such as polyimide resin, and two or more solder bumps 125 for electric shielding and the solder bump 127 for signal transmissions are arranged in the principal plane which faced the outside.
[0425] The base substrate 134 has two or more internal wiring 130 and 131 which connects electrically the solder bump 125 for electric shielding, and the solder bump 127 for signal transmissions to an internal configuration.
[0426] The internal wiring 130 and 131 is connected to the carrier film 124 arranged on the principal plane which turned to each inside the base substrate 134. The carrier film 124 has the electric wiring (a pad is included) and the glue line 133 which were arranged on the insulating film so that it may explain later. The electrical signal from the solder bump 127 for signal transmissions is transmitted to a semiconductor chip 122 through the chip electrode 132 linked to the pad of the internal wiring 130 and the carrier film 124. Moreover, a glue line 133 pastes up the carrier film 124 and a semiconductor chip 122. In addition, although not shown in drawing 54 , the carrier film 124 is pasted up by the glue line different also from the base substrate 134.
[0427] Moreover, in the interior of the base substrate 134, the electric shielding electrode 126 which consists of conductors is embedded. The plane view configuration of the electric shielding electrode 126 has structure with opening which can pass rectangle annular, without nothing and the internal wiring 130 contacting the electric shielding electrode 126. Drawing 54 is a sectional view in the location which cuts opening of the electric shielding electrode 126, and the broken line shows the opening concerned.
[0428] It is fixed to power-source potential or touch-down potential through the solder bump 125 for electric shielding, and the internal wiring 131, and the electric shielding electrode 126 can prevent that the internal wiring 130 gathers an external electric noise.
[0429] Moreover, electric shielding electrode 126b is arranged on the upper principal plane of the carrier film 124 so that a semiconductor chip 122 may be surrounded. A plane view configuration is a rectangle annular plate, it connects with the internal wiring 131 electrically through the electric wiring on the carrier film 124, and electric shielding electrode 126b is fixed to power-source potential or touch-down potential.
[0430] The stress relaxation film 135 is arranged so that electric shielding electrode 126b may be covered. The stress relaxation film 135 serves to ease the stress between a semiconductor chip 122 and the base substrate 134.
[0431] Although the cross-section configuration of the stress relaxation film 135 is originally a rectangle, it is inserted between the edge section of a semiconductor chip 122, and the carrier film 124, and while deforming, thickness becomes thin partially. That is, although stress concentrates on the part pinched by the edge section and the carrier film 124 of a semiconductor chip 122, stress is eased because thickness becomes thin.
[0432] Thermoplastic elastomer is used for the stress relaxation film 135. Although thermoplastic elastomer shows rubber elasticity in ordinary temperature, it is the polymeric materials which are plasticized at an elevated temperature and can perform various fabrication.
[0433] Moreover, an epoxy resin etc. is used for the binder of a semiconductor chip 122 and the stress relaxation film 135. To the coefficient of cubical expansion of thermoplastic elastomer being about 2.7x10-6, the coefficient of cubical expansion of silicon is about 3.1x10-6, and since the difference of a coefficient of cubical expansion is small, thermal stress can be eased.
[0434] In the semiconductor package, since there is a trouble of internal wiring becoming thin for a long

time, and becoming easy to gather a noise in order to reconcile increase of the number of terminals, and the miniaturization of a package, the electric shielding electrode 126 and the solder bump 125 for electric shielding are arranged. Moreover, the thermal stress between a semiconductor chip 122 and the base substrate 134 becomes large, and in order to prevent that the dependability of electrical installation falls, the stress relaxation film 135 is arranged.
[0435] The function of the electric shielding electrode 126 is as having mentioned above, and the electric shielding electrode 126 is connected to the solder bump 125 for electric shielding through the internal wiring 131. And the solder bump 125 for electric shielding is arranged so that the perimeter of the solder bump 127 for signal transmissions may be surrounded, and it has the function to prevent that the internal wiring 130 gathers an external electrical noise through the solder bump 127 for signal transmissions. In addition, although illustration is omitted, the solder bump 125 for electric shielding and the solder bump 127 for signal transmissions are connected to the mother board on which wiring was printed.
[0436] Moreover, in the former, MCP structure was realized only in QFP. The cross-section configuration of the MCP structure which used QFP for drawing 55 is shown. In drawing 55 , three semiconductor chips 102a, 102b, and 102c are accumulated and arranged in one package 107, and the closure is carried out by resin 106.
[0437] As an example, semiconductor chips 102a and 102c is [SRAM and semiconductor chip 102b] flash EEPROMs.
[0438] The internal wiring 109 connects between each semiconductor chip, and the electrical installation with the exterior is made with the external lead wire 113 through a bonding wire 112.
[0439] By considering as such a configuration, more memory space can be obtained to the same occupancy area rather than what has only one semiconductor chip in one package. So, there is much need to a Personal Digital Assistant.
[0440] However, compared with the chip area, the component-side product became large, and QFP had the trouble that external lead wire tends to gather a noise.
[0441] Thus, even if it made it CSP and made it QFP, there were merits and demerits, and since it will be necessary in MRAM to prevent further that the spin of a software ferromagnetic layer is reversed under the effect of an external magnetic field, the configuration of the conventional package was not employable as it was.
[0442] The configuration of MRAM2000 which starts the gestalt 8 of operation using drawing 56 - drawing 65 R> 5 is explained below a <H-2. equipment configuration>.
[0443] The flat-surface configuration which looked at the cross-section configuration of MRAM2000 to drawing 56 , and looked at MRAM2000 from the lower part side to drawing 57 is shown. In addition, drawing 56 shows the cross section in the A-A line in drawing 57 .
[0444] As shown in drawing 56 , the semiconductor chip 122 containing the circumference circuit and various functional block of a MRAM cel array is contained by the screen SHB of the cube type which consists of conductors of high permeability, such as a permalloy (nickel80Fe20).
[0445] As an ingredient of Screen SHB, super MAROI (Mo5nickel79Fe16) other than a permalloy may be used as the software ferromagnetic used for example, for a MRAM memory cell, and an EQC and the ferromagnetic which has bigger permeability than it. Since the ferromagnetic with large coercive force may work as a permanent magnet and a surrounding electrical machinery and apparatus may be affected, the small ferromagnetic of coercive force is desirable. The ferrite of a permalloy, super MAROI, and Mn50Zn50 grade is an ingredient which fulfills this condition.
[0446] The stress relaxation film 235 which consists of thermoplastic elastomer is arranged in the internal surface of Screen SHB. The stress relaxation film 235 serves to ease the stress of a semiconductor chip 122 and Screen SHB.
[0447] In the one side edge of the tubed outer frame section 237 from which Screen SHB serves as the body section, and the outer frame section 237, it is had and constituted and the stress relaxation film 235 is arranged [edge / the wrap up plate 238 and / of the outer frame section 237 / another side / plate / 236 / wrap lower] by the inside of the up plate 238 and the outer frame section 237.

[0448] Moreover, opening is prepared in the lower plate 236 and it has composition in which the internal wiring 130 connected to the semiconductor chip 122 penetrates the opening concerned.
[0449] As for a package 129, nothing and the screen SHB with the opening to the semiconductor chip 122 are inserted in box-like [of closed-end ****].
[0450] A package 129 is magnitude which contains Screen SHB and has still more spatial allowances, and the resin material 128 which consists of resin, such as an epoxy resin, is arranged between Screen SHB and the wall of a package 129.
[0451] Finally opening of a package 129 is covered by the base substrate 134. The body of the base substrate 134 concerned consists of insulating materials, such as polyimide resin, and two or more solder bumps 125 for electric shielding and the solder bump 127 for signal transmissions are arranged in the principal plane which faced the outside. In addition, the base substrate 134 is fixed by the adhesives applied to the carrier film 124 or the lower plate 236 grade.
[0452] The base substrate 134 has two or more internal wiring 130 and 131 which connects electrically the solder bump 125 for electric shielding, and the solder bump 127 for signal transmissions to an internal configuration.
[0453] The internal wiring 130 and 131 is arranged so that it may connect with the carrier film 124 arranged on the principal plane which turned to each inside the base substrate 134, and the internal wiring 131 is electrically connected to the lower plate 236 of Screen SHB through the pad and electric wiring which are arranged on the carrier film 124.
[0454] Moreover, the internal wiring 131 is electrically connected to the electric shielding electrode 126 which consists of conductors embedded to the interior of the base substrate 134. In addition, since some electric shielding electrodes 126 do not necessarily exist in the same cross section as the internal wiring 130 and 131, in drawing 56 , the broken line shows it.
[0455] In addition, the electric shielding electrode 126 is fixed to power-source potential or touch-down potential, and it serves for the internal wiring 130 to prevent gathering an external electric noise.
[0456] It connects with the pad (film electrode) prepared on the carrier film 124 directly, and the chip electrode 132 used as the input/output terminal of a semiconductor chip 122 is electrically connected to the internal wiring 130 through the film electrode and electric wiring by which patterning is carried out on the carrier film 124 concerned. In addition, the internal wiring 130 is connected to the solder bump 127 for signal transmissions.
[0457] The solder bump 127 for signal transmissions is a terminal for delivering and receiving an electrical signal with the semiconductor chip of the exterior and the interior, and the solder bump 125 for electric shielding is a terminal which fixes the potential of Screen SHB to touch-down potential.
[0458] Moreover, as shown in drawing 57 , the solder bump 125 for electric shielding is arranged so that the solder bump 127 for signal transmissions may be surrounded.
[0459] In addition, the solder bump 127 for signal transmissions and the solder bump 125 for electric shielding have the function which distributes the stress which joins the base substrate 134 to an installation substrate (mother board), and can reduce the stress which joins per solder bump by forming the solder bump 125 for electric shielding.
[0460] The outline of the mounting approach of MRAM2000 is explained using 2. In addition, drawing 58 - drawing 62 do not express correctly the configuration which shows the mounting approach of MRAM2000 typically and is shown in drawing 56 .
[0461] In drawing 58 , the carrier film 124 pasted the upper part of the base substrate 134, and the stress relaxation film 223 has pasted up on the carrier film 124.
[0462] The stress relaxation film 223 is arranged so that the arrangement field of the film electrode 219 in which rectangle annular was prepared by nothing and the carrier film 124 may be surrounded. Moreover, the rectangle annular slot 224 is formed in the stress relaxation film 223, and the lower plate 236 (drawing 56) of Screen SHB is arranged in the slot 224. In addition, the configuration in which the lower plate 236 was arranged in the slot 224 is shown in drawing 64 (a) and drawing 64 (b).
[0463] Moreover, although omitted, illustration is a next process, and the outer frame section 237 (drawing 46) of Screen SHB is arranged along a slot 224, and it is connected to the lower plate 236.

[0464] In addition, since the stress relaxation film 223 is making rectangle annular, in the direction of X and the direction of Y which are shown in drawing 58 , stress can be eased similarly.
[0465] The film electrode 219 arranged on the carrier film 124 which is an insulator is connected to the solder bump 127 for signal transmissions through the internal wiring 130.
[0466] In addition, connection between each bump and each chip electrode can be set as arbitration by carrying out patterning of the film electrode 219 on the carrier film 124, and the internal wiring 130 suitably.
[0467] The glue line 133 other than the film electrode 219 is alternatively arranged by the carrier film 124. A glue line 133 is for pasting up a semiconductor chip 122 with the carrier film 124.
[0468] Next, in the process shown in drawing 59 , each chip electrode of a semiconductor chip 122 carries a semiconductor chip 122 so that each film electrode of the carrier film 124 may be contacted, and it fixes a semiconductor chip 122 by the glue line 133.
[0469] Drawing 60 shows the condition of having reversed the base substrate 134 of the condition which shows in drawing 59 , and the semi-sphere solder bump formation hole 211 is arranged by the base substrate 134. The internal wiring 130 and 131 (refer to drawing 56) has reached the internal surface of the solder bump formation hole 211, and when a solder bump fills the inside of the solder bump formation hole 211 at a next process, a solder bump and the internal wiring 130 and 131 will be connected electrically. In addition, a conductive polymer may be used instead of a solder bump.
[0470] Drawing 61 shows the condition of having arranged the solder bump 127 for signal transmissions, and the solder bump 125 for electric shielding on the solder bump formation hole 211.
[0471] And after covering a semiconductor chip 122 by the screen SHB with the stress relaxation film 235 (drawing 56) inside, it inserts in the package 129 of closed-end ****, and as shown in drawing 62 , a configuration with the solder bump 127 for signal transmissions and the solder bump 125 for electric shielding is obtained at the rear face by pouring encapsulants, such as resin, into a clearance.
[0472] Here, the plane view configuration of the stress relaxation film 223 is explained to be the lower plate 236 which constitutes Screen SHB using drawing 63 , drawing 64 (a), and drawing 64 R> 4 (b). In addition, drawing 63 shows the cross-section configuration of the outline in the B-B line in drawing 56 , and drawing 64 (a) and drawing 64 (b) show the cross-section configuration in the C-C line and D-D line in drawing 63 R> 3.
[0473] As shown in drawing 63 , the lower plate 236 consists of plates of the rectangle which has the rectangular opening OP in the center, and the rectangle annular electric shielding electrode 126 (drawing 56) electrically connected to the solder bump 125 for electric shielding is arranged at the base substrate 134 side. in addition, the dimension of the electric shielding electrode 126 -- the dimension of the lower plate 236, and abbreviation -- it is the same.
[0474] In addition, since the stress relaxation film 223 is arranged in the inside and the outside of the opening edge of Screen SHB and the stress relaxation film 235 (refer to drawing 56) is arranged inside [whole] Screen SHB, the stress from the outside which joins a semiconductor chip 231 and a semiconductor chip 232 can be reduced.
[0475] Since the semiconductor chip 122 containing a MRAM cel array was surrounded by the screen SHB covered from an external magnetic field according to MRAM2000 concerning the gestalt 8 of the operation explained beyond the <H-4. operation effectiveness>, it can prevent that the spin of a MRAM cel is reversed with an external magnetic field, and the direction of magnetization, i.e., data, is rewritten.

[0476] Moreover, since the stress relaxation film 223 is arranged in the inside and the outside of the opening edge of Screen SHB and the stress relaxation film 235 is arranged inside Screen SHB, it can reduce that the deflection of the installation substrate (mother board) which attaches MRAM2000, and the stress from the outside resulting from a temperature cycle join a semiconductor chip 122.
[0477] <H-5. modification 1> In addition, in MRAM2000 explained above, although the semiconductor chip to mount was shown as one, it is good like MRAM2100 shown in drawing 65 also as a configuration which lays semiconductor chip 122b (magnetic storage chip) containing a MRAM cel array on semiconductor chip 122a (circuit chip) in which the circumference circuit and various

functional block of a MRAM cel array were contained.
[0478] Semiconductor chip 122a equips both principal planes with a chip electrode, and semiconductor chip 122a and semiconductor chip 122b are connected by the film electrode and electric wiring on carrier film 124b arranged among both. Moreover, adhesion immobilization of semiconductor chip 122a and the semiconductor chip 122b is carried out by the glue line 133.
[0479] In addition, since electric connection with semiconductor chip 122a and the solder bump 127 for signal transmissions is the same as connection with the semiconductor chip 122 and the solder bump 127 for signal transmissions who show drawing 65 and it is fundamentally [as MRAM2000] the same except the point that the carrier film 124 is carrier film 124a, explanation is omitted.
[0480] Moreover, semiconductor chip 122a and semiconductor chip 122b may arrange vertical relation conversely. In that case, what is necessary is just to arrange a chip electrode in both sides of semiconductor chip 122b.
[0481] Moreover, the combination of the arbitration of a well-known semiconductor chip is [that the MRAM cel array should just be arranged by the chip of the method of one at least] possible for the combination of semiconductor chip 122a and semiconductor chip 122b.
[0482] In MRAM2100 shown in drawing 65 , since semiconductor chip 122a in which the circumference circuit and various functional block of a MRAM cel array were contained, and semiconductor chip 122b containing a MRAM cel array are manufactured separately and combined, it is not necessary to take the difference in formation temperature into consideration, and each formation temperature can be optimized. And since semiconductor chips 122a and 122b are manufactured separately, a production process advances to parallel and production time can be shortened.
[0483] In MRAM2000 shown in <H-6. modification 2> drawing 56 , although the ferromagnetic was used for the ingredient of Screen SHB instead, even if it uses the antiferromagnetic substance, such as IrMn 20-30atom.% Containing Ir (iridium), the same effectiveness is done so.
[0484] Moreover, Screen SHB may consist of multilayers of ferromagnetic 136a and antiferromagnetic substance 136b like MRAM2200 shown in drawing 66 . In that case, let similarly the electric shielding electrode 126 in the base substrate 134 be the multilayers of ferromagnetic 126a and antiferromagnetic substance 126b. In addition, the vertical relation of multilayers is not limited above.
[0485]
[Effect of the Invention] According to the magnetic storage according to claim 1 concerning this invention, since the easy axis whose at least one magnetic tunnel junction is the easy direction of magnetization of a software ferromagnetic layer is arranged so that it may have the include angle of 40 - 45 degrees to the extension direction of two or more bit lines and two or more word lines, with few write-in currents, it can reverse the direction of magnetization of a software ferromagnetic layer certainly, and can reduce the power consumption at the time of writing.
[0486] Since according to the magnetic storage according to claim 2 concerning this invention it is constituted by the rectangle so that the side parallel to an easy axis may become longer than the side which intersects perpendicularly with an easy axis in the plane view configuration of a magnetic tunnel junction, it can prevent that it becomes easy to define an easy axis and an easy axis changes with the anisotropies resulting from a configuration.
[0487] according to the magnetic storage according to claim 3 concerning this invention -- the 1st and 2nd change means -- the 1st and 2nd edges of a bit line -- the 1st -- since it can change and connect with the power source of a certain **** 2, a bidirectional current can be passed to a bit line, the direction of magnetization of a magnetic tunnel junction is changed to it, and it becomes it the writing of data, and eliminable.
[0488] According to the magnetic storage according to claim 4 concerning this invention, since the 1st and 2nd change means are constituted from the 1st of the same conductivity type - the 4th MOS transistor, manufacture becomes easy.
[0489] According to the magnetic storage according to claim 5 concerning this invention, the 1st change means is constituted from the 1st and 2nd MOS transistors of conductivity types differing. Since the 2nd change means is constituted from the 3rd and 4th MOS transistors from which a conductivity type

differs On the other hand, the 1st and 2nd MOS transistors reach, and the burden which it becomes unnecessary to apply the electrical potential difference more than supply voltage to one control electrode of the 3rd and 4th MOS transistors in an ON state, and starts gate dielectric film can be made small.
[0490] According to the magnetic storage according to claim 6 concerning this invention, between the 1st [of the 1st and 2nd MOS transistors] main electrode, Since it has the 5th and 6th MOS transistor which will always be in an ON state between the 1st [of the 3rd and 4th MOS transistors] main electrode, respectively The stress electrical potential difference which joins one 1st main electrode of the 1st and 2nd MOS transistors and one 1st main electrode of the 3rd and 4th MOS transistors is reduced, the leakage current resulting from a stress electrical potential difference is reduced, and power consumption can be reduced.
[0491] Since the number of the memory cell directly connected to the same wiring by using two or more main word lines crossed to two or more memory cell arrays and the word line only over a single memory cell array in the magnetic storage which has two or more memory cell arrays decreases according to the magnetic storage according to claim 7 concerning this invention, load-carrying capacity is reduced. Consequently, the time delay resulting from load-carrying capacity can be shortened, and rapid access can be realized.
[0492] Since the number of the memory cell directly connected to the same wiring by using the word line only on magnetic storage equipped with two or more memory cell array groups which have two or more memory cell arrays, and over a single memory cell array, two or more main word lines crossed to two or more memory cell arrays, and two or more global word lines crossed to two or more memory cell array groups according to the magnetic storage according to claim 8 concerning this invention decreases, load-carrying capacity is reduced. Consequently, the time delay resulting from load-carrying capacity can be shortened, and rapid access can be realized.
[0493] Since the number of the memory cell directly connected to the same wiring by using two or more Maine bit lines crossed to two or more memory cell arrays and the bit line only over a single memory cell array in the magnetic storage which has two or more memory cell arrays decreases according to the magnetic storage according to claim 9 concerning this invention, load-carrying capacity is reduced. Consequently, the time delay resulting from load-carrying capacity can be shortened, and rapid access can be realized.
[0494] Since the number of the memory cell directly connected to the same wiring by using the bit line only on magnetic storage equipped with two or more memory cell array groups which have two or more memory cell arrays, and over a single memory cell array, two or more Maine bit lines crossed to two or more memory cell arrays, and two or more global bit lines crossed to two or more memory cell array groups according to the magnetic storage according to claim 10 concerning this invention decreases, load-carrying capacity is reduced. Consequently, the time delay resulting from load-carrying capacity can be shortened, and rapid access can be realized.
[0495] Since package elimination or the package writing of the data of two or more memory cells which have at least one magnetic tunnel junction can be carried out by having the inductor which generates a field in the direction in alignment with the easy axis which is the easy direction of magnetization of a software ferromagnetic layer according to the magnetic storage according to claim 11 concerning this invention, processing in a short time is attained.
[0496] According to the magnetic storage according to claim 12 concerning this invention, since a field is efficiently generated by the coiled form inductor, there is little power consumption in the case of package-eliminating or package writing in the data of two or more memory cells, and it ends.
[0497] Since package elimination or the package writing of the data of two or more memory cells which have at least one magnetic tunnel junction can be carried out by equipping the outside of two or more bit lines and two or more word lines of at least one memory cell array with a flash plate bit line and a flash plate word line, and passing the current of the predetermined direction to these according to the magnetic storage according to claim 13 concerning this invention, processing in a short time is attained.
[0498] According to the magnetic storage according to claim 14 concerning this invention, in the magnetic storage with which two or more memory cell arrays were arranged in the shape of a matrix,

since a flash plate bit line and a flash plate word line can also carry out package elimination or the package writing of the data of two or more memory cell arrays, the processing of them in a short time is attained by arranging so that a matrix may be constituted in accordance with the array of two or more memory cell arrays.
[0499] Since it has at least one inductor which saves the current of the selected bit line and a word line which flows to the method of one at least by LC resonance, and at least one capacitor according to the magnetic storage according to claim 15 concerning this invention, a write-in current can be recycled and the power consumption at the time of writing can be reduced.
[0500] According to the magnetic storage according to claim 16 concerning this invention, the concrete configuration for recycling the write-in current in a bit line can be obtained.
[0501] According to the magnetic storage according to claim 17 concerning this invention, the concrete configuration for recycling the write-in current in a word line can be obtained.
[0502] According to the magnetic storage according to claim 18 concerning this invention, it can prevent that the direction of magnetization of a magnetic tunnel junction is reversed with an external magnetic field, and data are rewritten in two or more memory cells containing at least one magnetic tunnel junction by containing at least one semiconductor chip to the electric shielding inside of the body which consists of conductors.
[0503] According to the magnetic storage according to claim 19 concerning this invention, since at least one semiconductor chip is held with the 1st and 2nd stress relaxation film, the stress from the outside can reduce joining two or more semiconductor chips.
[0504] dividing into a magnetic storage chip and a circuit chip including the circumference circuit of a memory cell array according to the magnetic storage according to claim 20 concerning this invention -- both -- it will manufacture separately, it is not necessary to take the difference in formation temperature into consideration, and each formation temperature can be optimized. Moreover, a production process advances to parallel and production time can be shortened.
[0505] According to the magnetic storage according to claim 21 concerning this invention, to a software ferromagnetic layer, or since a screen consists of ferromagnetics which have bigger permeability than it, it can cover an external magnetic field effectively.
[0506] According to the magnetic storage according to claim 22 concerning this invention, since a screen consists of the antiferromagnetic substance, it can cover an external magnetic field effectively.
[0507] According to the magnetic storage according to claim 23 concerning this invention, since a screen consists of multilayers of a ferromagnetic and the antiferromagnetic substance, it can cover an external magnetic field effectively.
[0508] Since it has at least the multilayers which form at least one magnetic tunnel junction arranged throughout the principal plane according to the magnetic-substance substrate according to claim 24 concerning this invention, when manufacturing the magnetic storage equipped with the memory cell which has at least one magnetic tunnel junction, a mere semi-conductor substrate can be prepared, a production process can be skipped compared with the case where multilayers are formed on the principal plane, and a manufacturing cost can be reduced.
[0509] According to the magnetic-substance substrate according to claim 25 concerning this invention, the magnetic-substance substrate suitable for manufacture of the magnetic storage equipped with the memory cell which has single MAG tunnel association is obtained.
[0510] According to the magnetic-substance substrate according to claim 26 concerning this invention, the semi-conductor substrate suitable for manufacture of the magnetic storage which equipped the lower part of single MAG tunnel association with the memory cell with pn junction diode is obtained.
[0511] Since at least one magnetic tunnel junction will be formed on the SOI substrate which can reduce the parasitic capacitance of MOSFET according to the magnetic-substance substrate according to claim 27 concerning this invention, the working speed of MOSFET can be made quick and a magnetic-storage working speed can also be made quick as a result.

[Translation done.]

* NOTICES *

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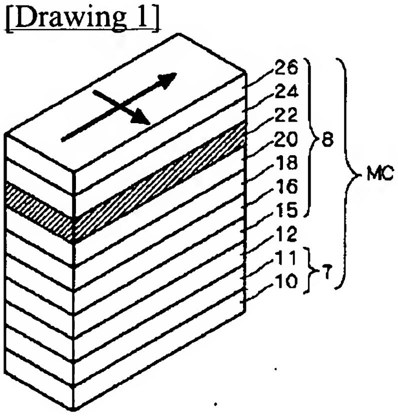
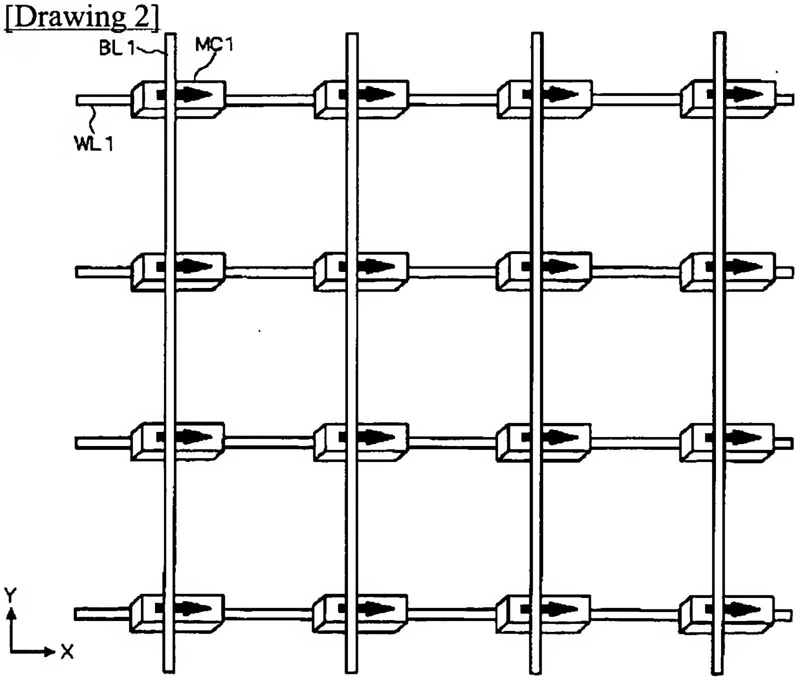
1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

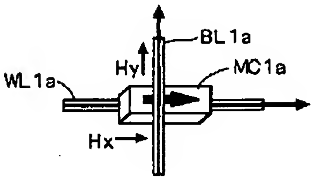
[Drawing 1]



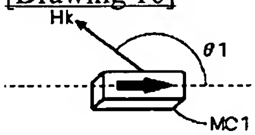
[Drawing 2]



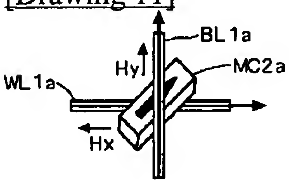
[Drawing 9]



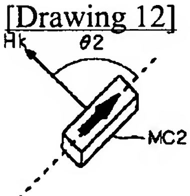
[Drawing 10]



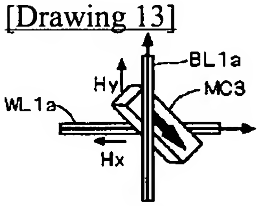
[Drawing 11]



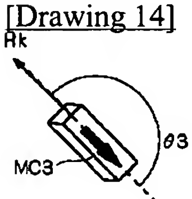
[Drawing 12]



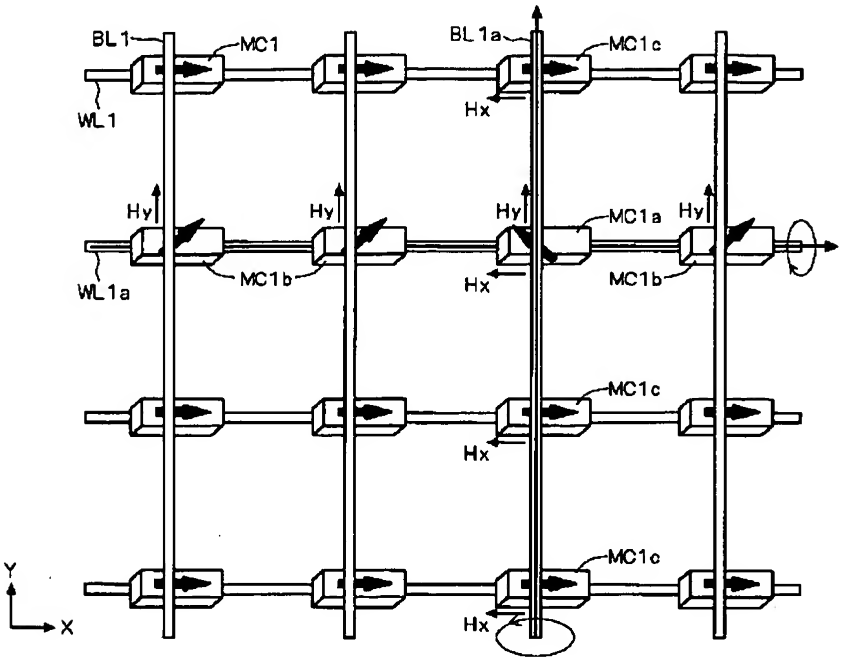
[Drawing 13]



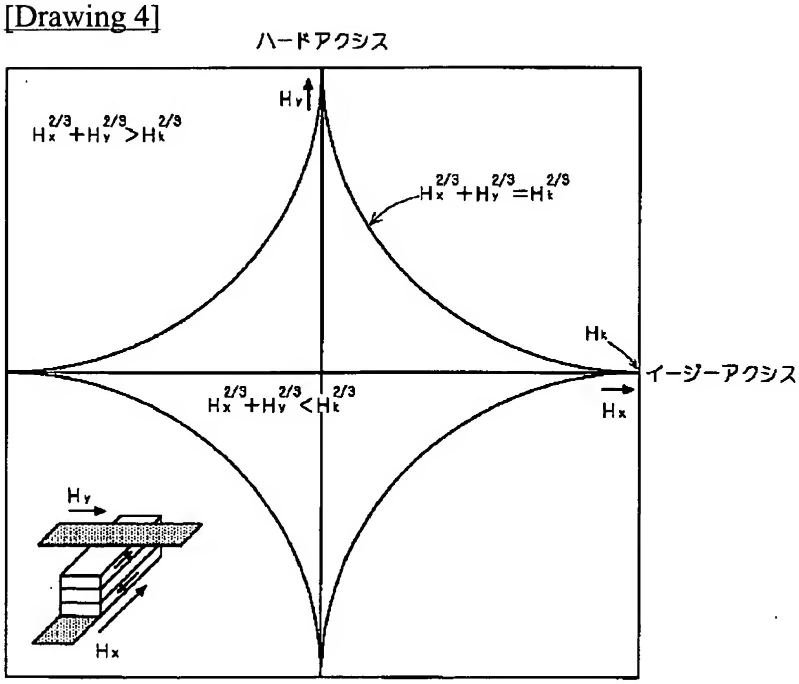
[Drawing 14]



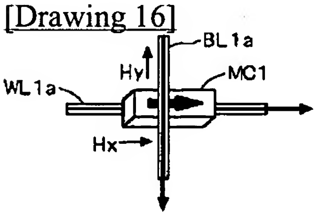
[Drawing 3]



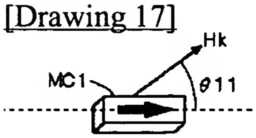
[Drawing 4]



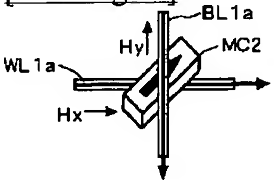
[Drawing 16]



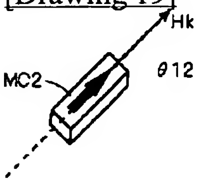
[Drawing 17]



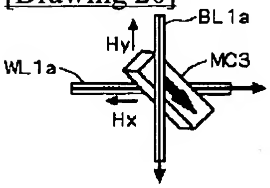
[Drawing 18]



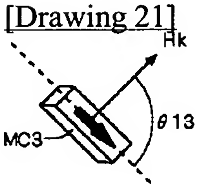
[Drawing 19]



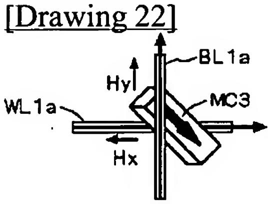
[Drawing 20]



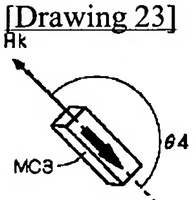
[Drawing 21]



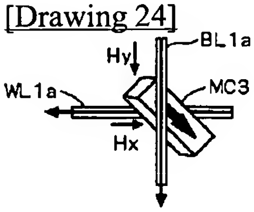
[Drawing 22]



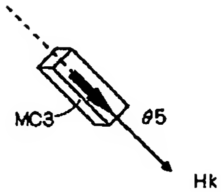
[Drawing 23]



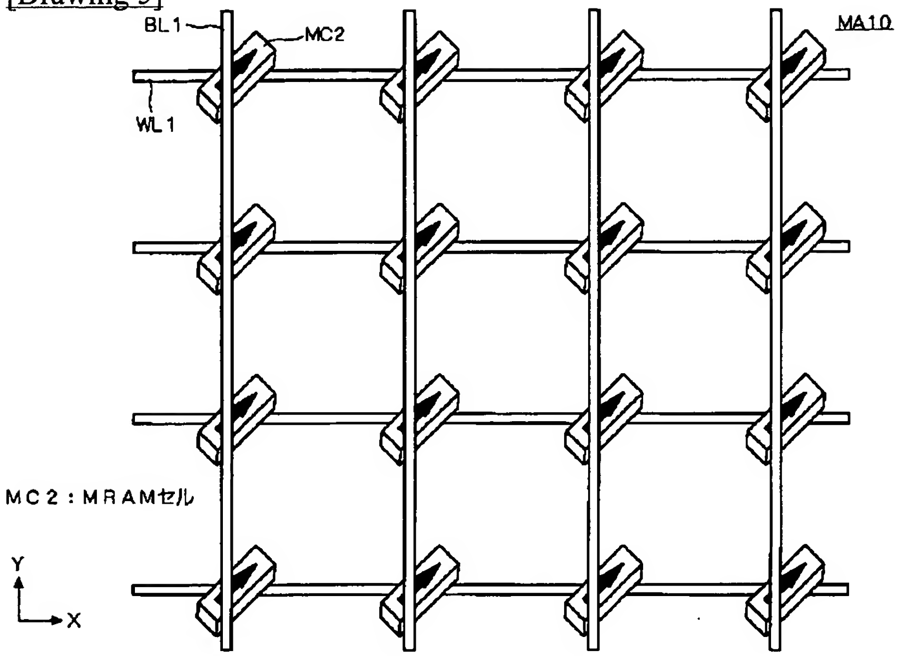
[Drawing 24]



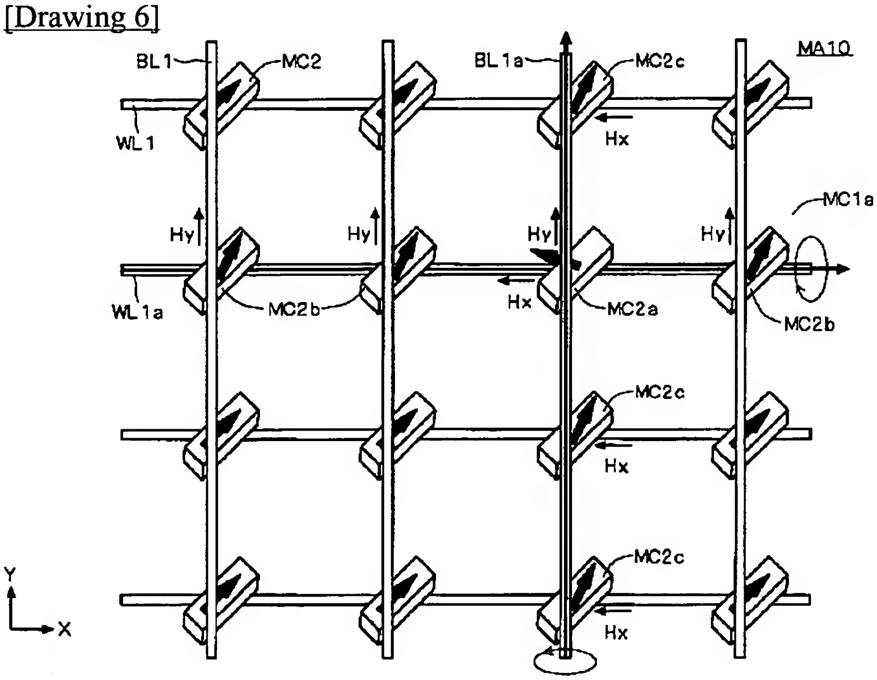
[Drawing 25]



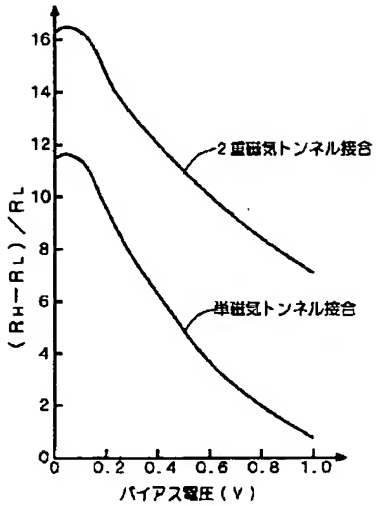
[Drawing 5]



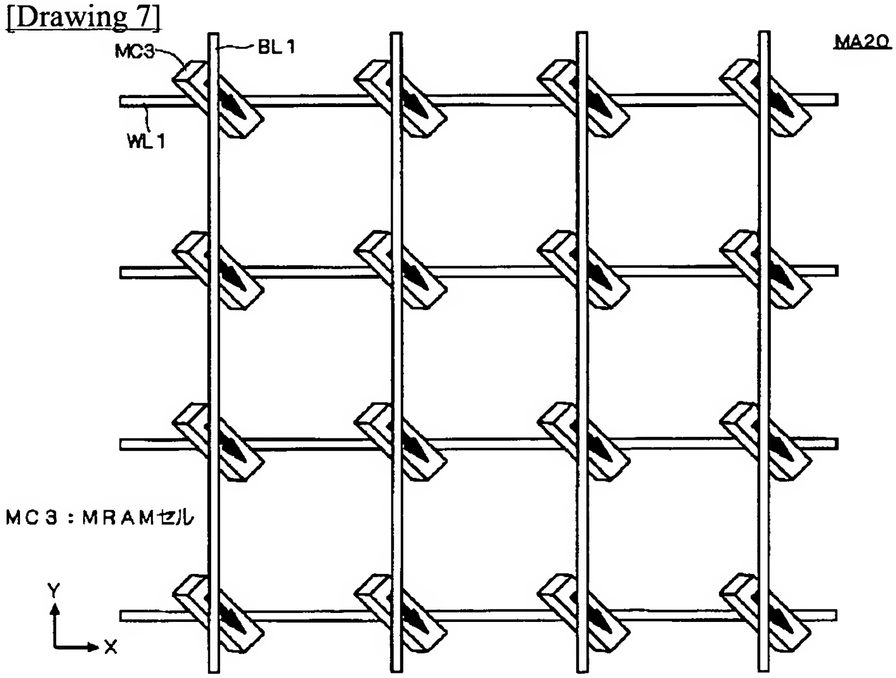
[Drawing 6]



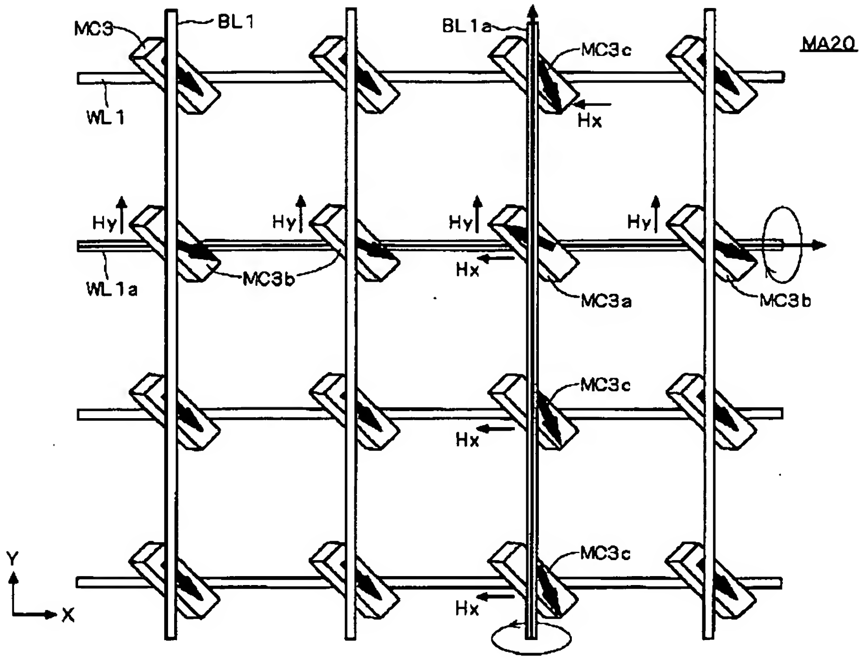
[Drawing 29]



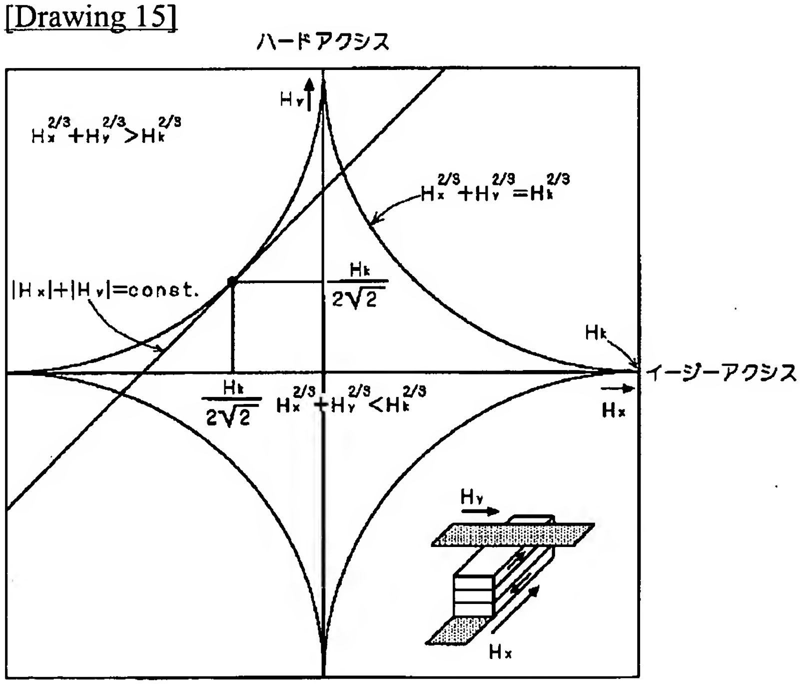
[Drawing 7]



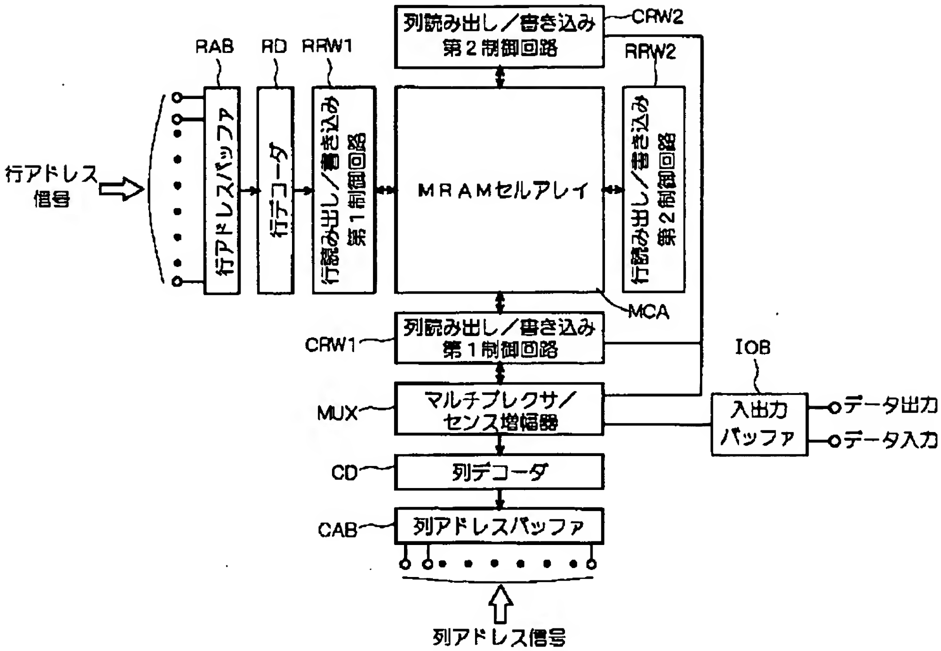
[Drawing 8]



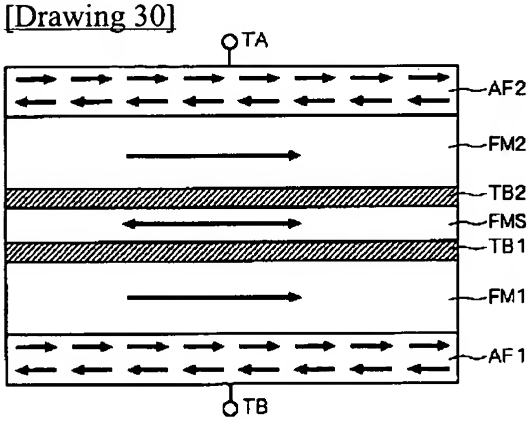
[Drawing 15]



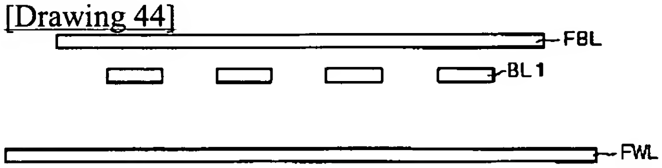
[Drawing 26]



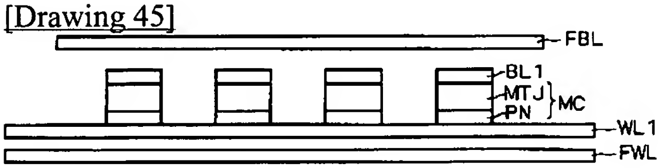
[Drawing 30]



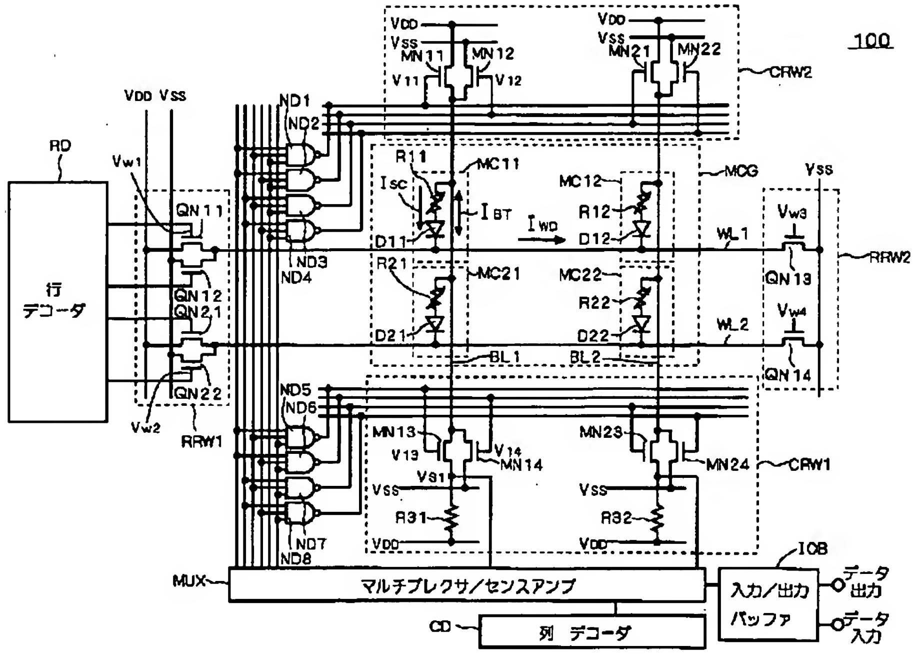
[Drawing 44]



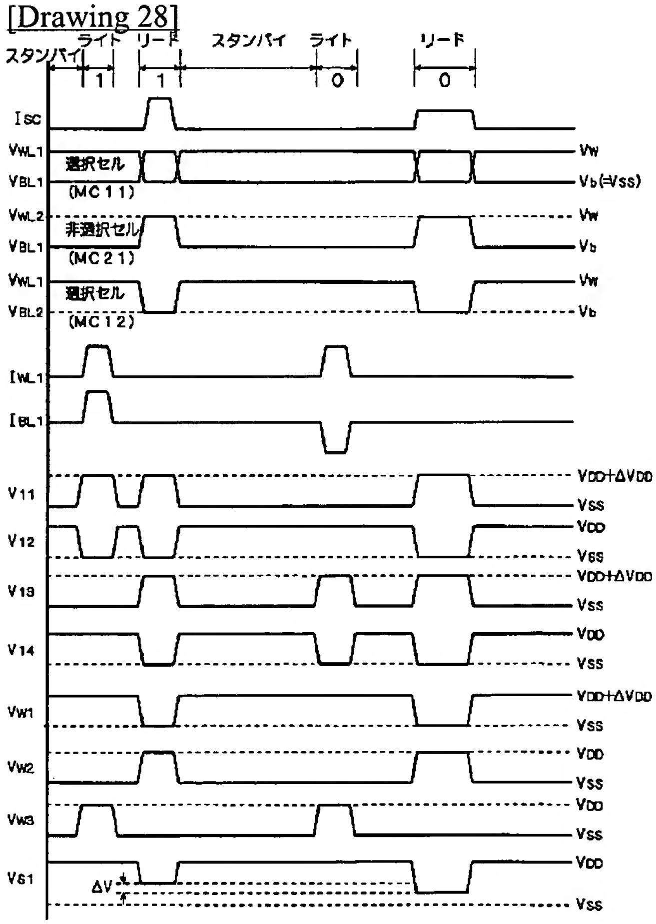
[Drawing 45]



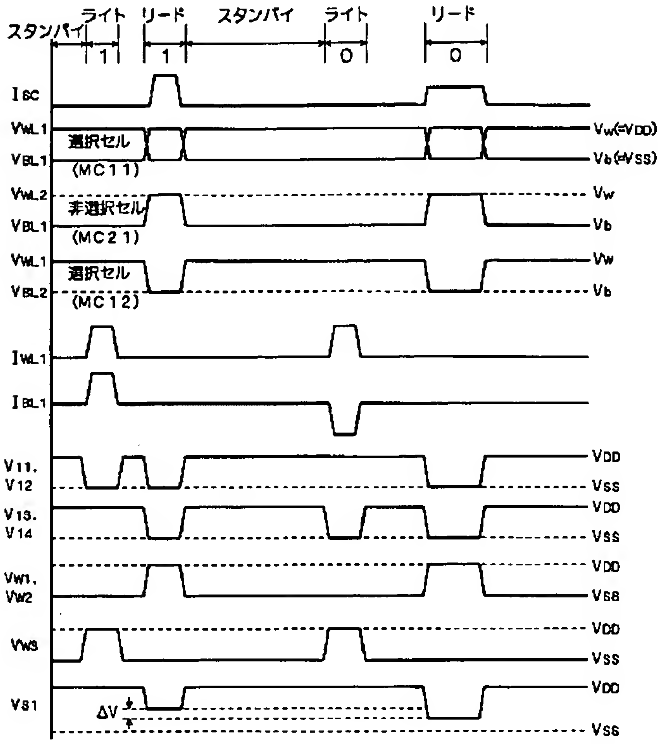
[Drawing 27]



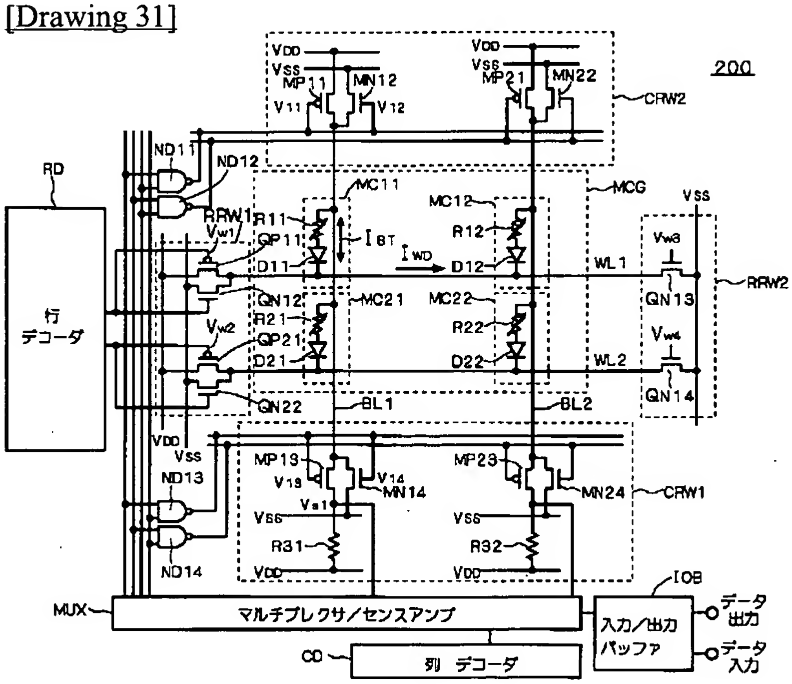
[Drawing 28]



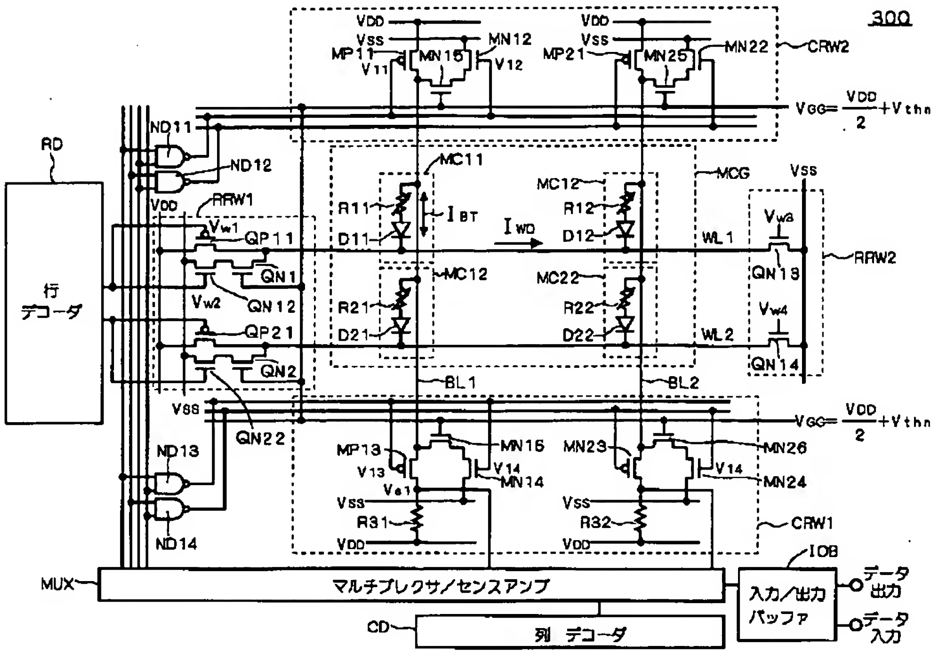
[Drawing 32]



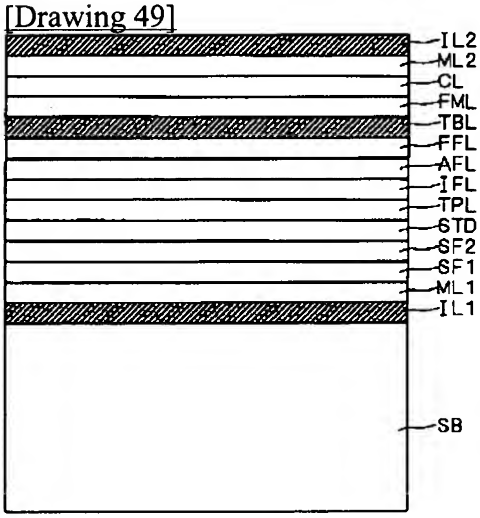
[Drawing 31]



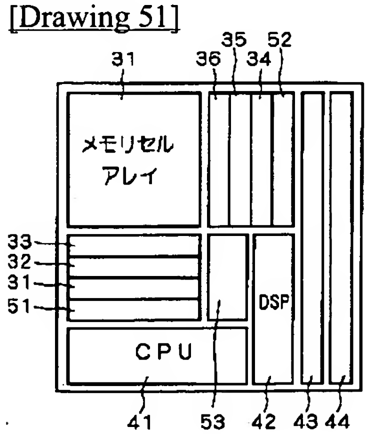
[Drawing 33]



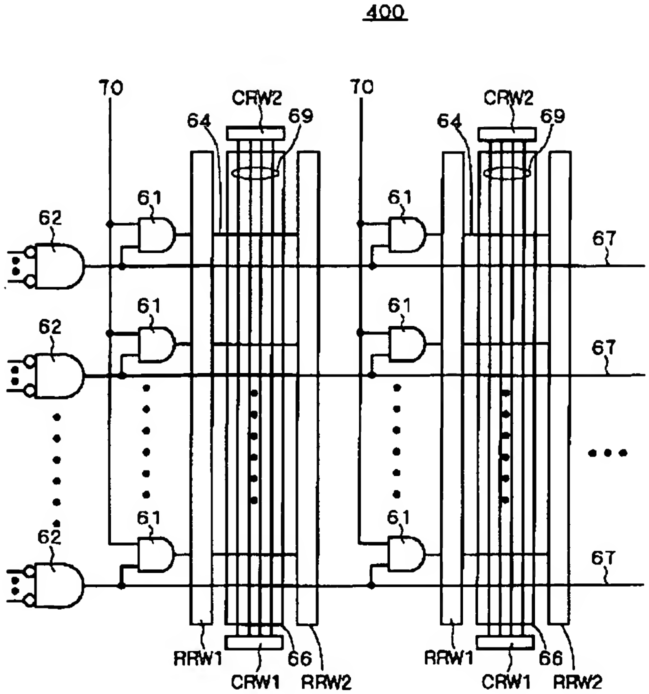
[Drawing 49]



[Drawing 51]

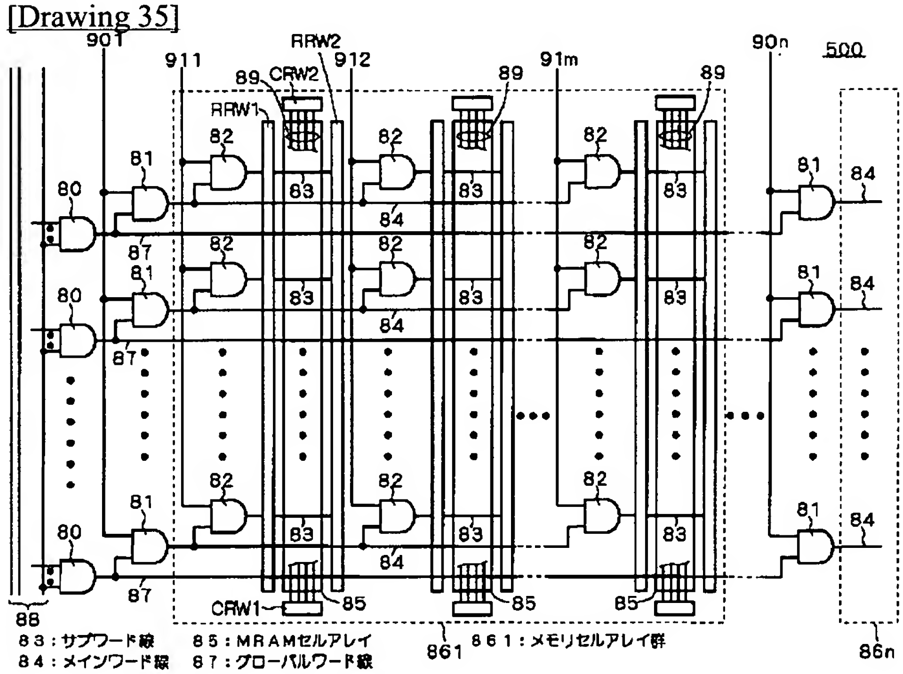


[Drawing 34]

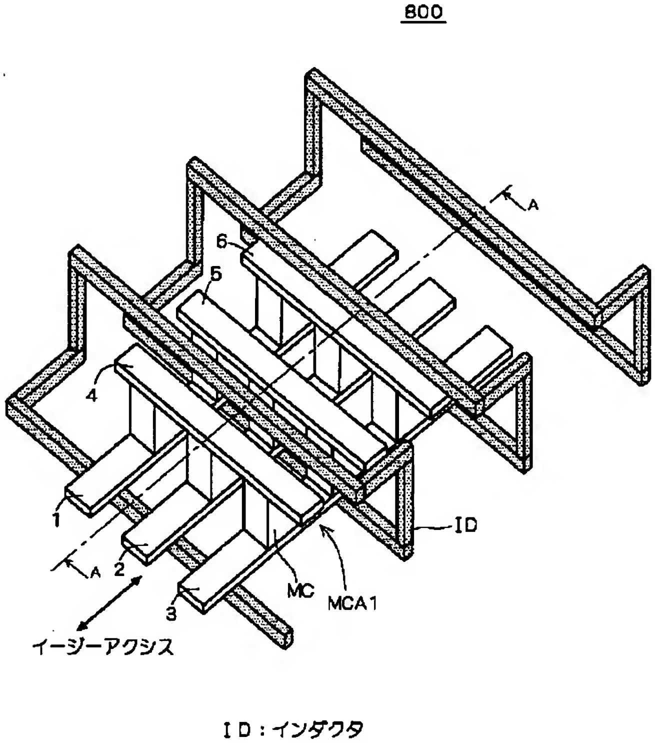


６４：サブワード線　６６：ＭＲＡＭセルアレイ
６７：メインワード線

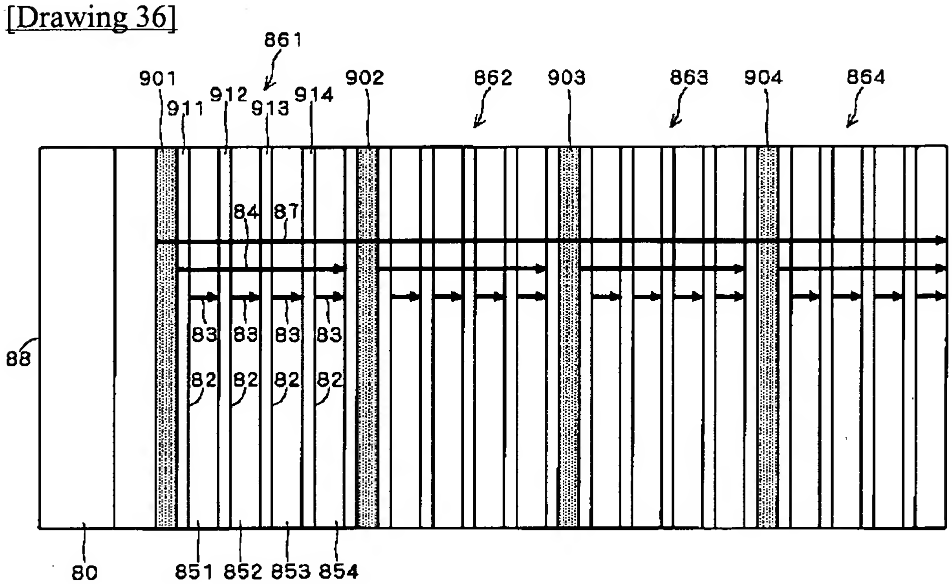
[Drawing 35]



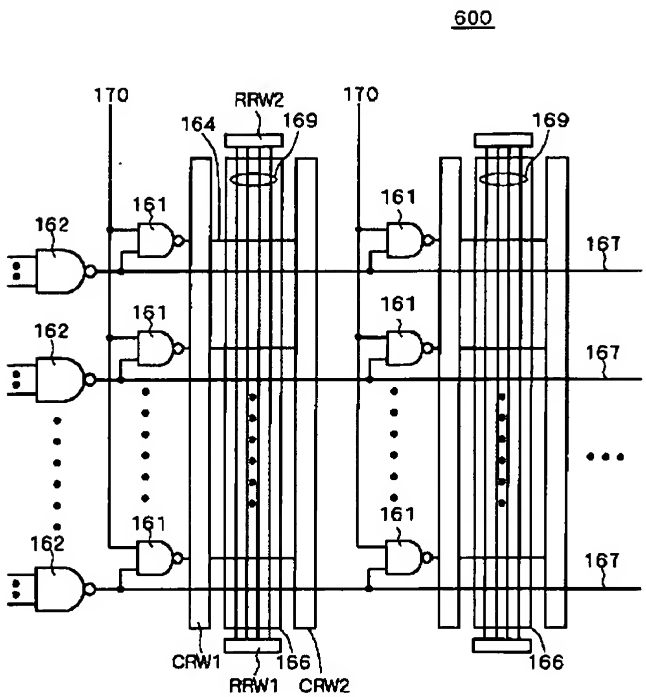
[Drawing 39]



[Drawing 36]

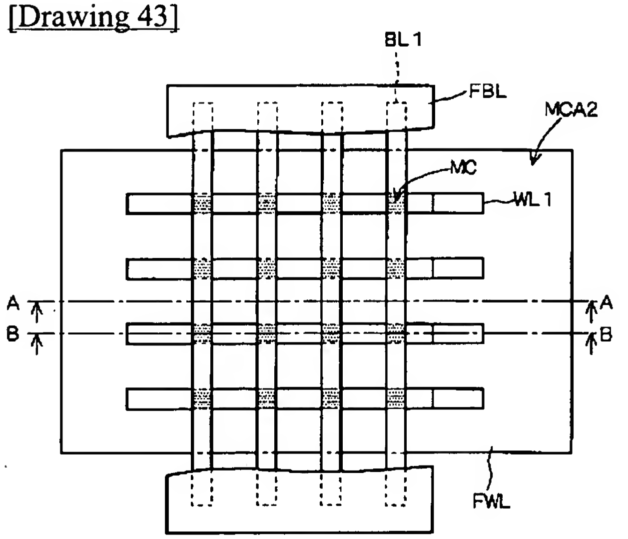


[Drawing 37]



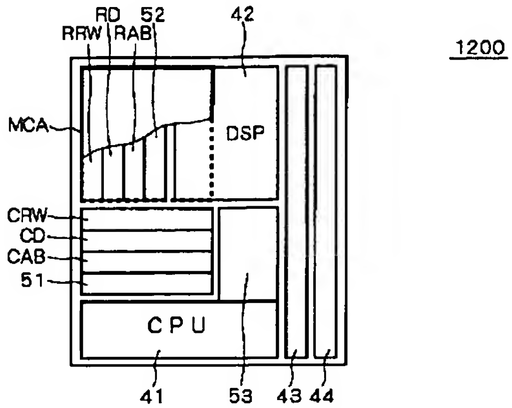
１６４：サブビット線
１６７：メインビット線
１６６：ＭＲＡＭセルアレイ

[Drawing 43]

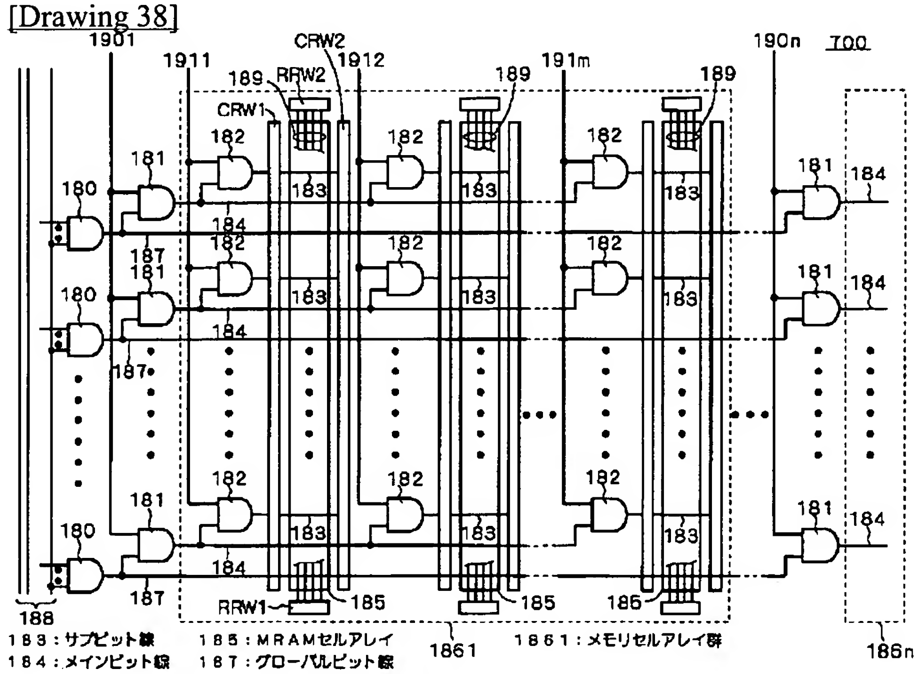


ＦＢＬ：フラッシュビット線
ＦＷＬ：フラッシュワード線

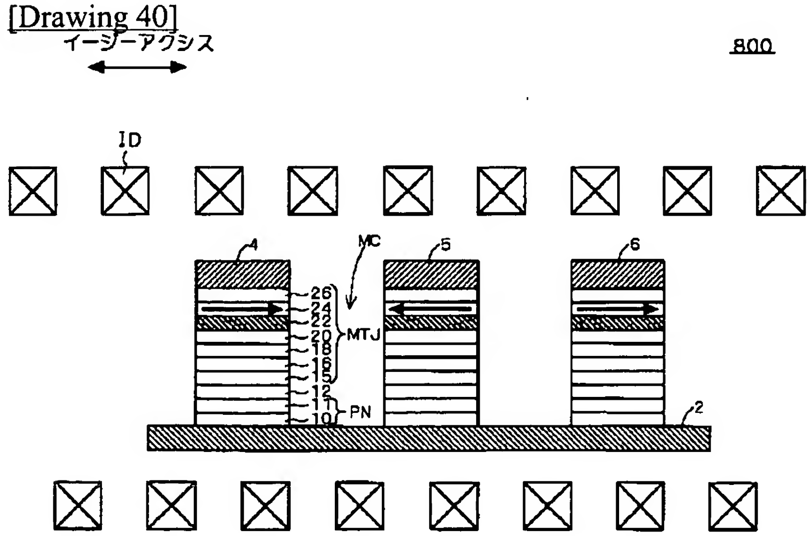
[Drawing 52]



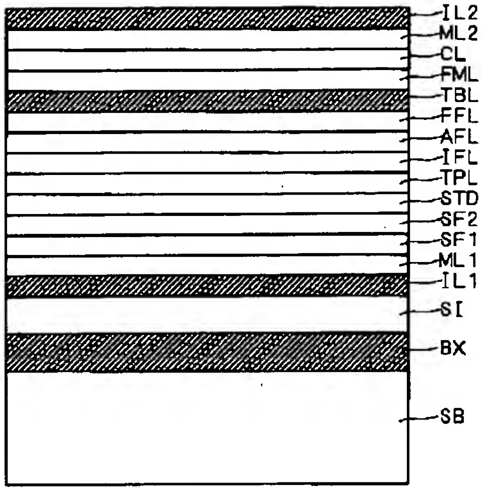
[Drawing 38]



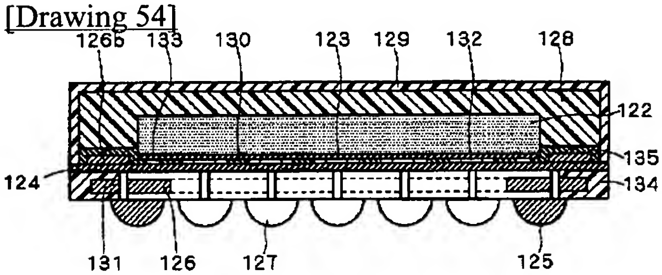
[Drawing 40]



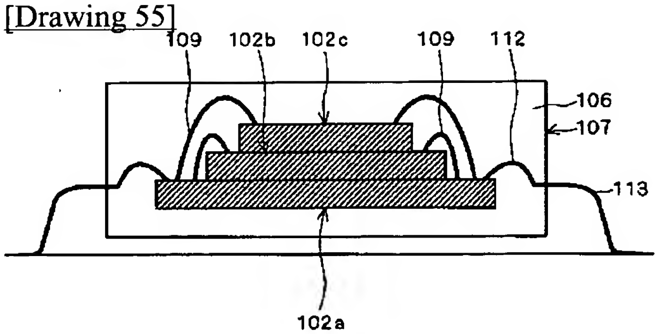
[Drawing 50]



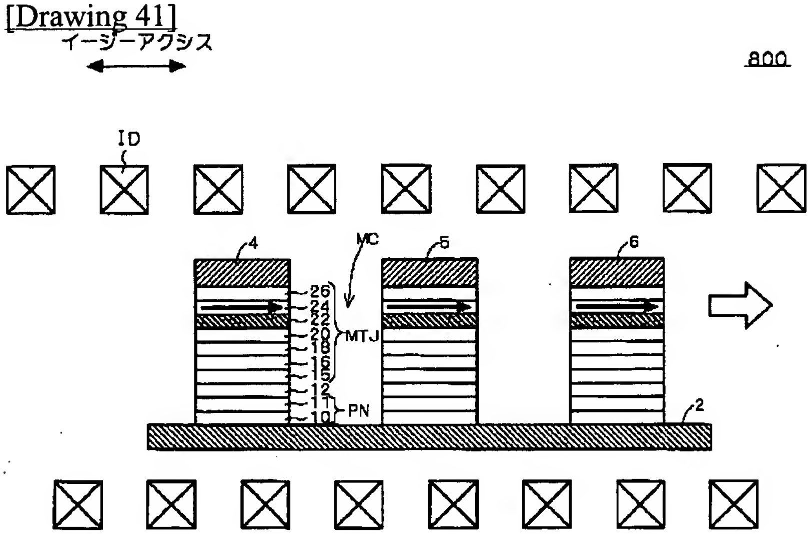
[Drawing 54]



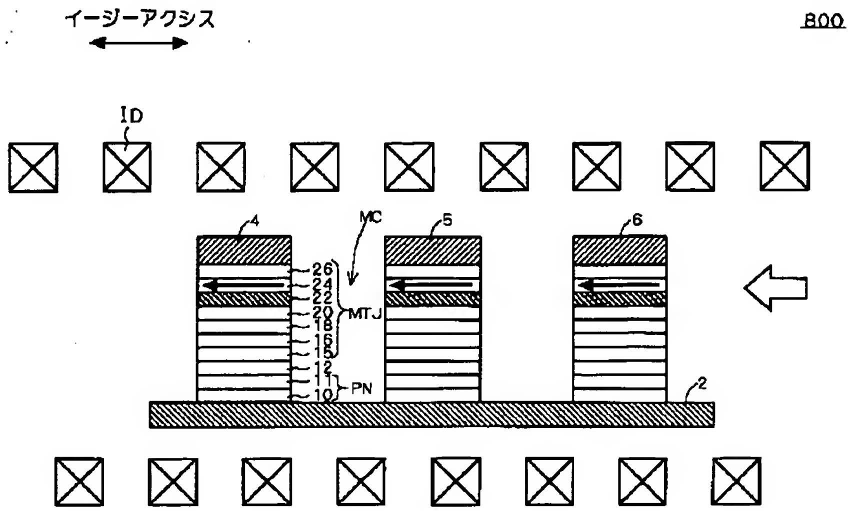
[Drawing 55]



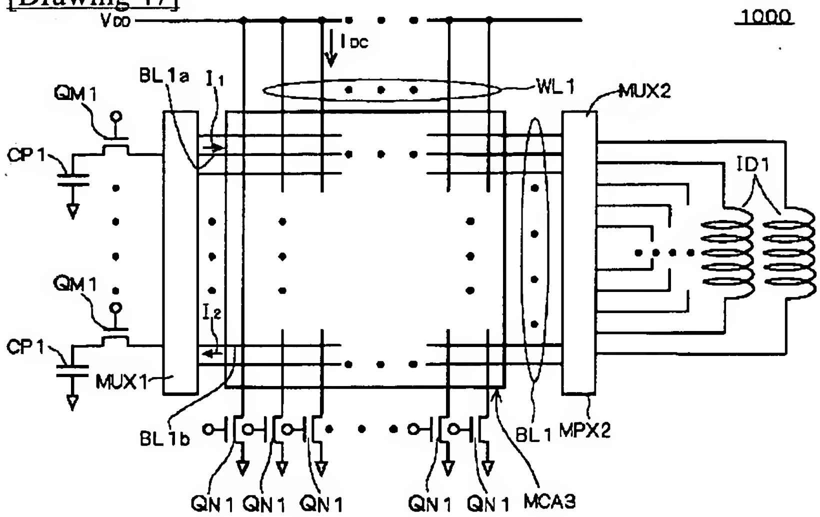
[Drawing 41]



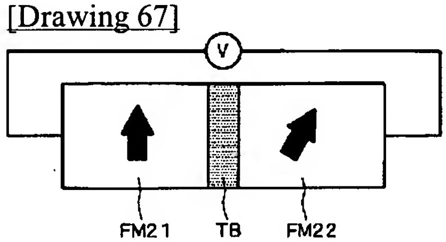
[Drawing 42]



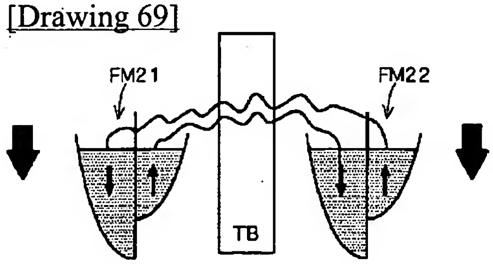
[Drawing 47]



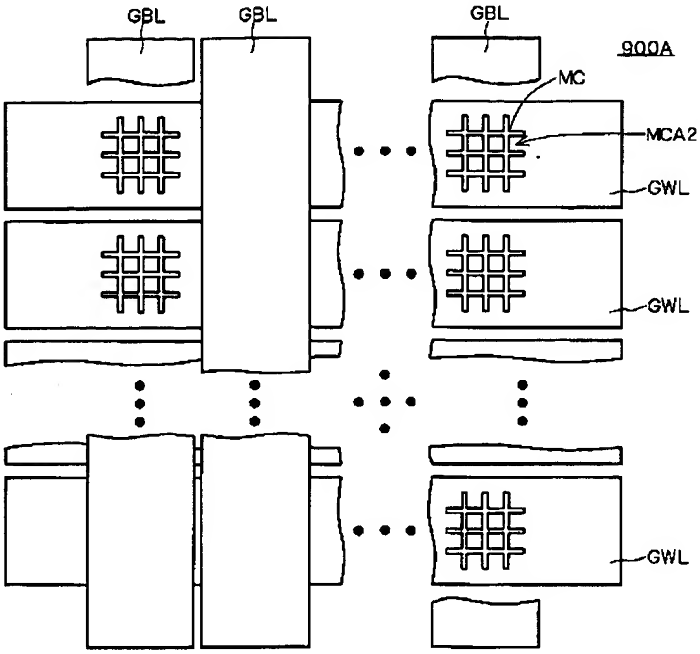
[Drawing 67]



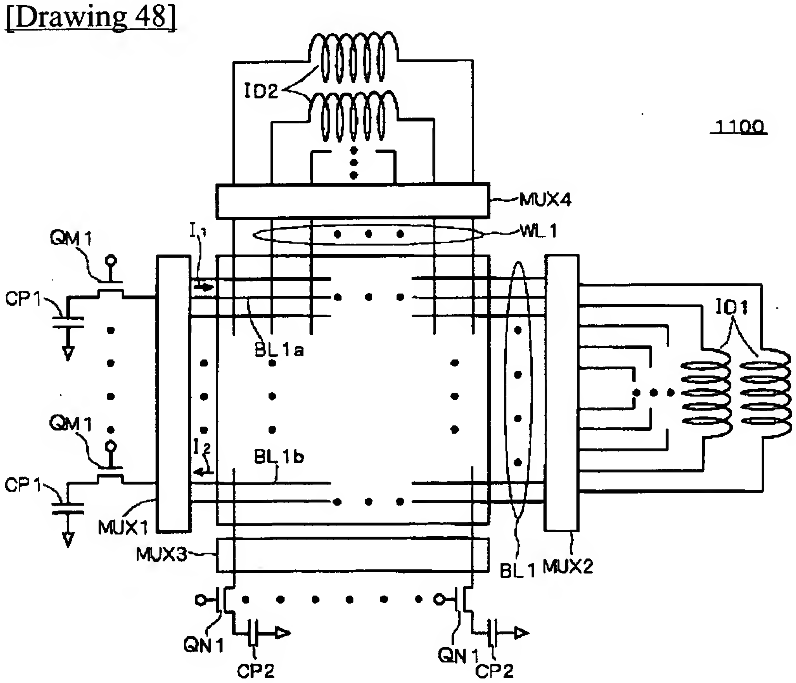
[Drawing 69]



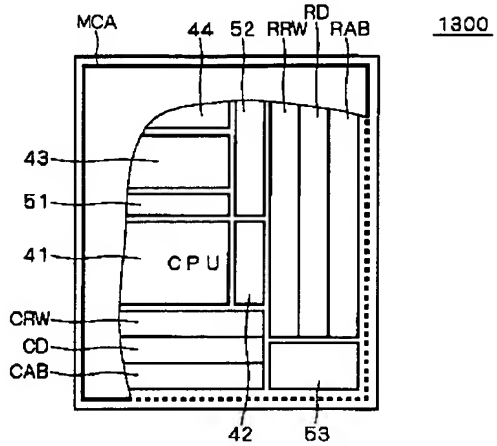
[Drawing 46]



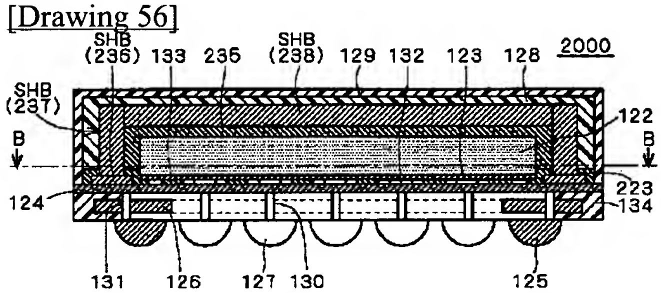
[Drawing 48]



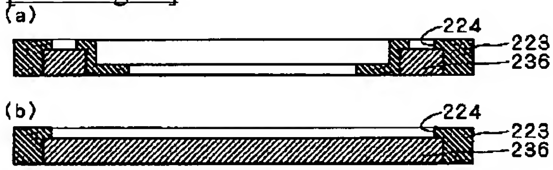
[Drawing 53]



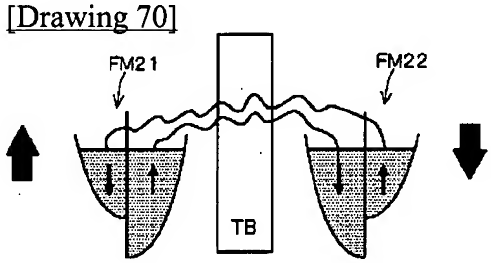
[Drawing 56]



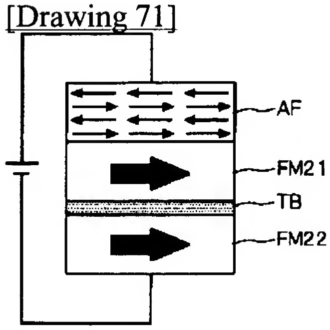
[Drawing 64]



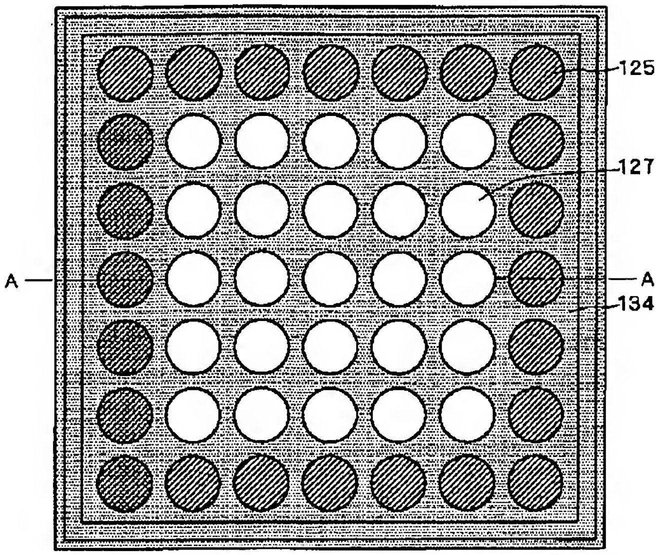
[Drawing 70]



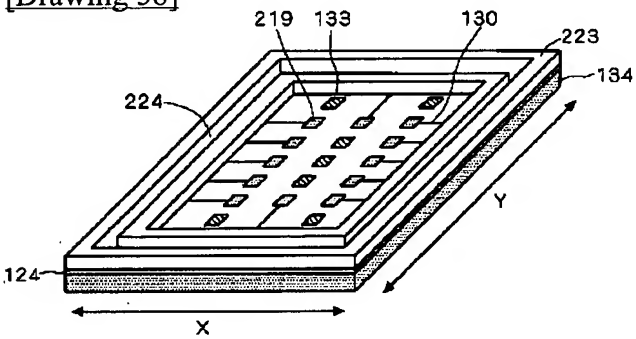
[Drawing 71]



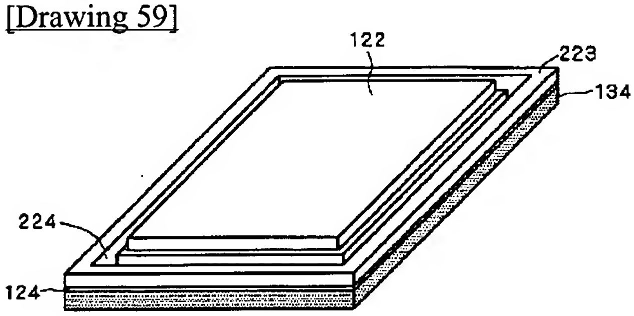
[Drawing 57]



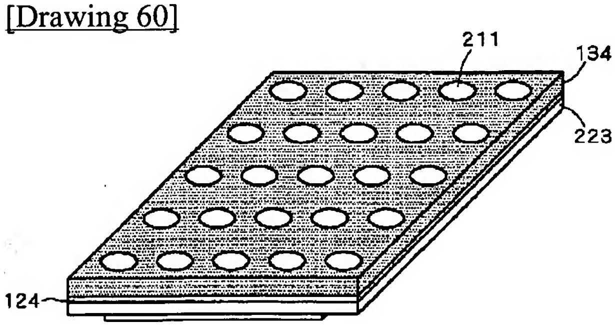
[Drawing 58]



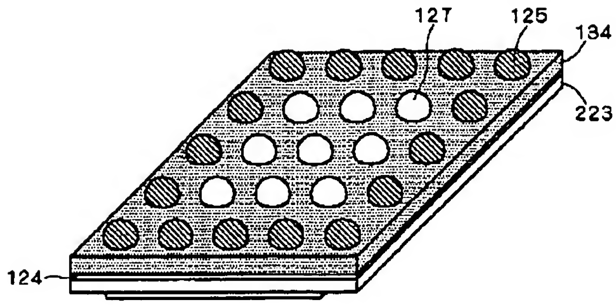
[Drawing 59]



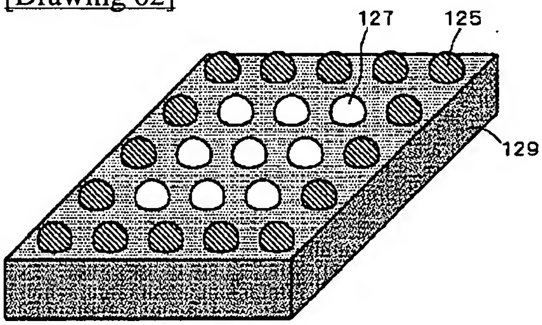
[Drawing 60]



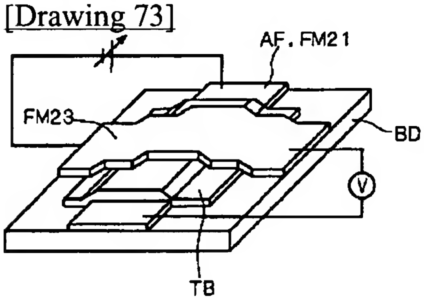
[Drawing 61]



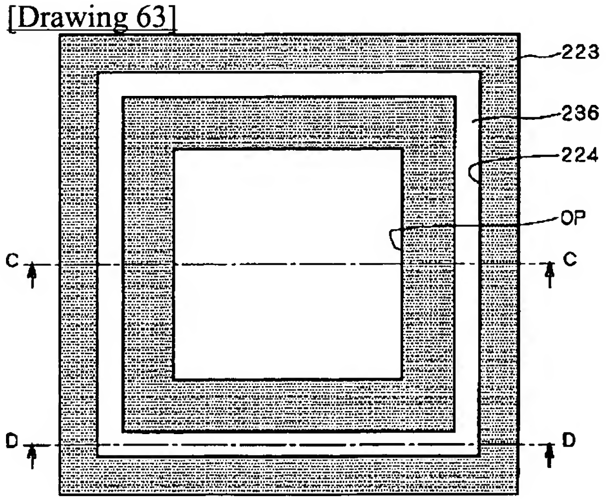
[Drawing 62]



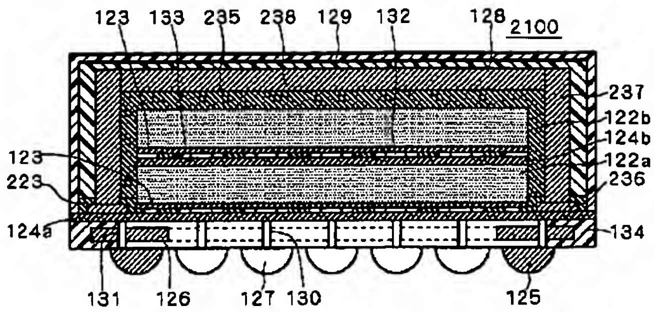
[Drawing 73]



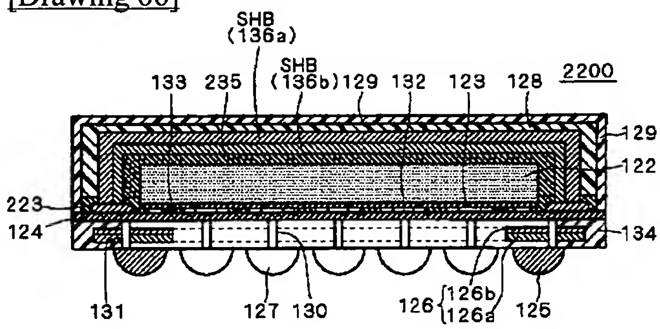
[Drawing 63]



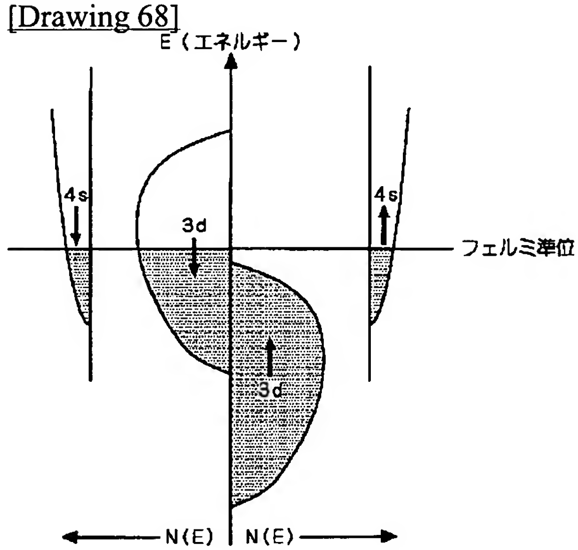
[Drawing 65]



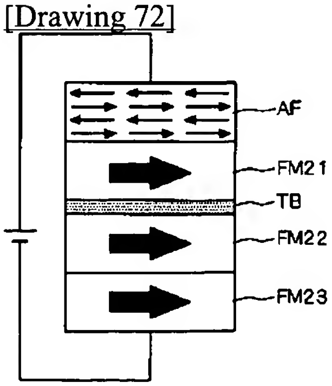
[Drawing 66]



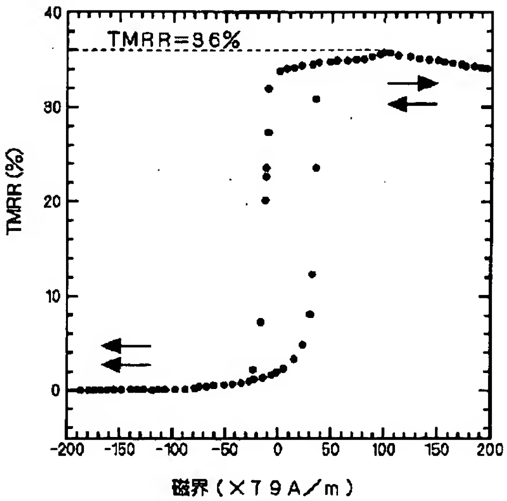
[Drawing 68]



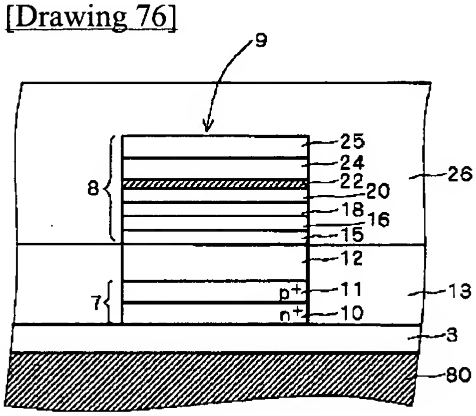
[Drawing 72]



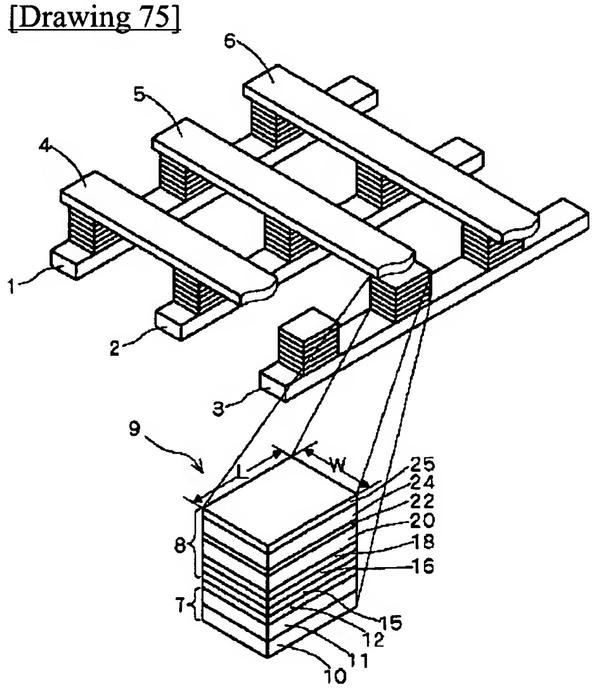
[Drawing 74]



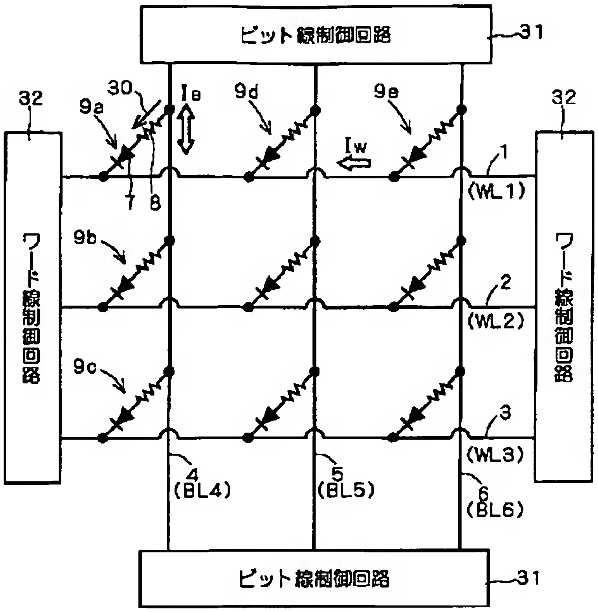
[Drawing 76]



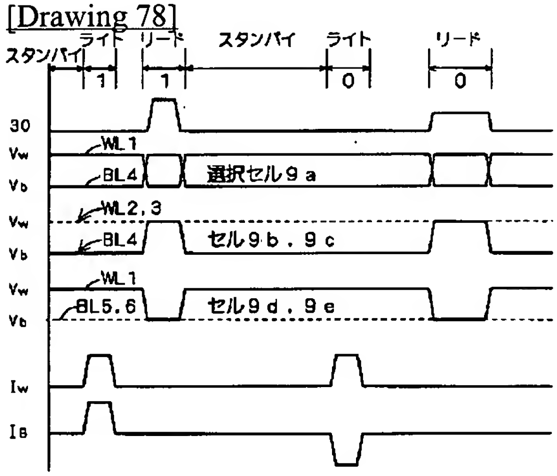
[Drawing 75]



[Drawing 77]



[Drawing 78]



[Translation done.]